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The Semiconductor Supply Chain: Assessing National Competitiveness

CSET Issue Brief

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Executive Summary

Advanced computer chips drive economic and scientific advancement as well as military capabilities. Complex supply chains produce these chips, and the global distribution of these chains and associated capabilities across nations have major implications for future technological competition and international security. However, supply chain complexity and opaqueness make it difficult to formulate policy. Avoiding unpredicted harms requires detailed understanding of the complete supply chain and national competitiveness across each element of that chain.

To help policymakers understand global semiconductor supply chains, we have broken down these supply chains into their component elements and identified the features most relevant to policymakers because they either offer potential targets for technology controls or constrain the policy options available. A companion CSET issue brief titled "U.S. Semiconductor Exports to China: Current Policies and Trends" provides an overview of how export controls are currently applied to semiconductor supply chains.[1] Companion CSET policy briefs titled "Securing Semiconductor Supply Chains"[2] and "China's Progress in Semiconductor Manufacturing Equipment"[3] offer policy recommendations based on the analysis in this paper to sustain U.S. and allied advantages.

The United States and its allies are global semiconductor supply chain leaders, while China lags. The U.S. semiconductor industry contributes 39 percent of the total value of the global semiconductor supply chain. U.S.-allied nations and regions—Japan, Europe (especially the Netherlands, the United Kingdom, and Germany), Taiwan, and South Korea—collectively contribute another 53 percent. Together, these countries and regions enjoy a competitive advantage in virtually every supply chain segment. While contributing only 6 percent, China is quickly developing capabilities across many segments and could attempt to reconfigure supply chains in its favor, impacting national and international security.

At a high level, semiconductor supply chains include research and development, production, production inputs, and distribution for end-use. R&D underpins all production and its inputs. Semiconductor production includes three segments: (1) design, (2) manufacturing, and (3) assembly, testing, and packaging (ATP). Production relies on associated elements of the supply chain: semiconductor manufacturing equipment (SME), materials

(including "wafers" formed into chips), design software (called electronic design automation, or EDA, software), and intellectual property related to chip designs (called core IP). The highest value and most technologically complex parts of this process are the design and fabrication segments of production, and the SME element of the supply chain. Although small elements, EDA and core IP are also critical and involve great expertise. ATP is labor-intensive and has the lowest barriers to entry.

The United States and its allies specialize in different supply chain segments. The United States dominates R&D and has strong capabilities across all segments. However, it lacks firms in certain key subsectors, especially photolithography tools (the most expensive and complex form of SME) and the most advanced chip factories (especially "foundries," which manufacture chips for third parties). South Korea specializes in all production steps, but also produces significant amounts of materials and some SME. Taiwan is dominant in the most advanced manufacturing and ATP, and produces some materials. By contrast, Japan specializes in SME and materials, and it produces many older technology semiconductors. Europe (especially the Netherlands, the United Kingdom, and Germany), meanwhile, specializes in SME (especially photolithography tools), materials, and core IP.

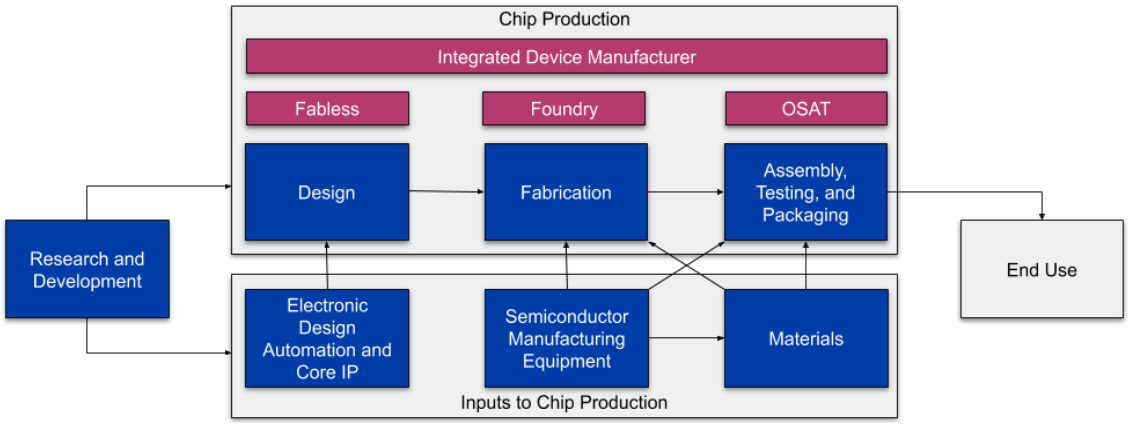
China has made progress in some segments, but struggles in others. China is strongest in ATP, tools for assembly and packaging, and raw materials. It is progressing in design and manufacturing, albeit with the help of state support. However, China struggles in production inputs: SME, EDA, core IP, and certain materials used in manufacturing.

Introduction and Overview

The half-trillion-dollar semiconductor supply chain[4] is one of the world's most complex. The production of a single computer chip often requires more than 1,000 steps passing through international borders 70 or more times before reaching an end customer.[5] However, the advancement of China's semiconductor industry could reconfigure these supply chains, affecting international security and the competitiveness of current incumbents. Policies that affect even a single firm or supply chain step can have global ripple effects with tens of billions of dollars of impact. To avoid unpredicted harms, policymakers must understand the supply chain and national competitiveness across each sector. This report aims to provide such an assessment. Though it maps national competitiveness for all key countries and regions, it focuses on China's development in each sector. Except where otherwise noted, data throughout this report is current as of 2019, and country and region market shares are based on firm headquarters, rather than locations of operations. However, firm headquarters may not fully capture national competitiveness. For example, many U.S. firms keep significant operations in China and other countries.

At a high level, the supply chain includes seven sectors (Figure 1).[6]

Figure 1: The semiconductor supply chain



Note: Blue: Supply chain segment; Purple: Business model for production

Research and development advances all sectors of the supply chain. It includes pre-competitive, exploratory research on foundational technologies and competitive research directly advancing the leading edge of semiconductor technology.

Production takes three major steps: **design**, **fabrication**, and **assembly, testing, and packaging** (ATP). These steps either occur in a single firm—an **integrated device manufacturer** (IDM) that sells the chip—or in separate firms, where a **fabless** firm designs and sells the chip and purchases fabrication services from a **foundry** and ATP services from an **outsourced semiconductor assembly and test** (OSAT) firm. Production requires several inputs: **materials**, **semiconductor manufacturing equipment** (SME), **electronic design automation** (EDA), and **core intellectual property** (IP). The following is a summary of production steps and how they use these inputs.

Design involves specification, logic design, physical design, and validation and verification. Specification determines how the chip should operate in the system using it.[7] Logic design creates a schematic model of interconnected electrical components. Physical design translates this model to a physical layout of electrical components and interconnects, the wires that connect components. Validation and verification ensure chips based on the design will operate as expected.[8] **EDA** is software used to design chips. Until the 1970s, when chips included few electric components, engineers drew designs manually. Today, chips include billions of interconnected transistors and other electrical components. To manage this complexity, chip designers use EDA software's automated design tools.[9] **Core IP** consists of reusable modular portions of designs,[10] allowing design firms to license and incorporate them in their designs.

Fabrication turns designs into chips, relying on various **SME** and **materials**. First, a furnace forms a cylinder of silicon (or other semiconducting materials), which is then cut into disc-shaped wafers (first image in Figure 2). Semiconductor fabrication facilities ("fabs") make chips in these wafers in two steps: forming transistors and other electrical devices in material layers within the silicon; and forming metal interconnects between the electrical devices in insulating layers above the silicon.[11] Together, the electrical devices and interconnects form circuits. A chip may contain dozens of layers in total. What follows is an example of how to form a single layer. First, "deposition" tools add a film of material that will form the basis of a new permanent layer. Then, a process called "photolithography" draws circuit patterns in the layer, starting with coating a "photoresist" on the deposited material. A photolithography tool passes light through a "photomask"—a transparent plate with a circuit pattern—to transfer that pattern to the photoresist. (Photomasks are themselves made with lithography tools.) The light dissolves

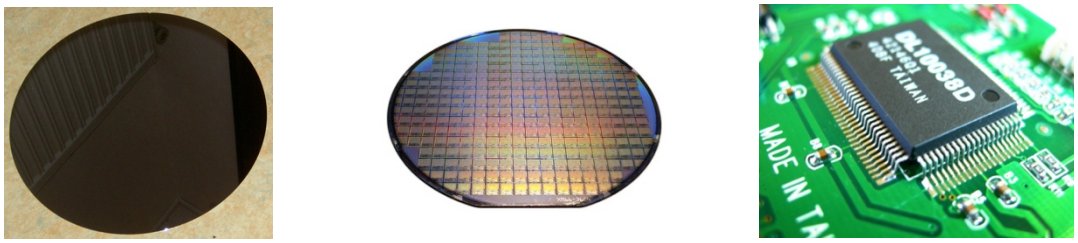
parts of the photoresist according to the circuit pattern. "Etching" tools carve the newly created pattern in the photoresist into the permanent layer below the photoresist. The photoresist is subsequently removed and the etched material cleaned off of the layer. (Other times, instead of etching, atoms are embedded into the layer in a process called "ion implantation.") Then, the completed layer is flattened (in a process called "chemical mechanical planarization") to allow a new layer to be added, and the process begins again.[12] Throughout fabrication, "process control" tools inspect the wafer and its layers to ensure no errors.

Assembly, testing, and packaging starts with cutting a finished wafer—which contains dozens of chips in a grid pattern after fabrication (second image in Figure 2)—into separate chips. Each chip is mounted on a frame with wires that connect the chip to external devices, and enclosed in a protective casing. This produces the final look of a dark gray rectangle with metal pins at the edges (third image in Figure 2). The chip is also tested to ensure it operates as intended. ATP also requires various **SME** and **materials**.

The above description oversimplifies the technical process, but conveys the high-level steps involved. In reality, each individual step is highly complex, requiring several sub-steps. And the atomic precision of the fabrication process requires clean rooms clear of dust particles, which can interfere with chip fabrication.

End use involves distribution of chips for integration into products—smartphones, laptops, servers, communications equipment, and automobiles, among others.[13]

Figure 2: The chip manufacturing process



New wafer → **Chips fabricated in wafer** → **Packaged chip**

Firms headquartered in six countries and regions control virtually the entire supply chain. Table 1 presents CSET estimates of the contribution to semiconductor value of each supply chain segment (in purple). These values

add to 100 percent. See Appendix A for calculations of value add for each supply chain segment. It also presents regional market shares of supply chain segments (in green). Table 1 also provides each region's total value add to the global supply chain (in blue). Each of these values is a weighted average of a region's market shares across all supply chain segments. The weighting is each segment's weighted by sectoral value add. Because of lack of data, Table 1 excludes fab materials besides wafers (4.1 percent value add), and packaging materials (3.5 percent value add). The former are typically purchased by fabs; the latter by ATP facilities. For this reason, the value of non-wafer fab materials and packaging materials are incorporated into "fab" and "ATP," respectively. The United States is the world leader overall, while South Korea, Japan, Taiwan, and Europe (especially the Netherlands, U.K., and Germany) contain world-leading firms in other advanced segments.

Table 1: Semiconductor value add and market shares by segment and firm headquarters

	Segment Value add	Market shares						
		U.S.	S. Korea	Japan	Taiwan	Europe	China	Other
EDA	1.5%	96%	<1%	3%	0%	0%	<1%	0%
Core IP	0.9%	52%	0%	0%	1%	43%	2%	2%
Wafers	2.5%	0%	10%	56%	16%	14%	4%	0%
Fab tools	14.9%	44%	2%	29%	<1%	23%	1%	1%
ATP tools	2.4%	23%	9%	44%	3%	6%	9%	7%
Design	29.8%	47%	19%	10%	6%	10%	5%	3%
Fab	38.4%	33%	22%	10%	19%	8%	7%	1%
ATP	9.6%	28%	13%	7%	29%	5%	14%	4%
Total value add		**39%**	**16%**	**14%**	**12%**	**11%**	**6%**	**2%**

Sources: CSET calculations, financial statements, WSTS, SIA, SEMI, IC Insights, Yole, and VLSI Research[14]
Note: Color intensities are correlated with the magnitude of the values.

The United States is strong in most segments (Table 2). Noteworthy exceptions include the production of some fab tools such as lithography equipment and materials including wafers. The United States also lacks leading-edge pure-play logic foundries. (A foundry is a fab that makes chips

for third-party customers, unlike U.S.-based Intel, whose leading-edge logic fabs make chips based on Intel's own chip designs.) However, these capabilities are all dominated by U.S. allies. Taken together, the United States and its allies are internationally competitive in every segment in the supply chain—in short, adding allies would turn all of Table 2 green.

Table 2: The United States' competitiveness across supply chain segments

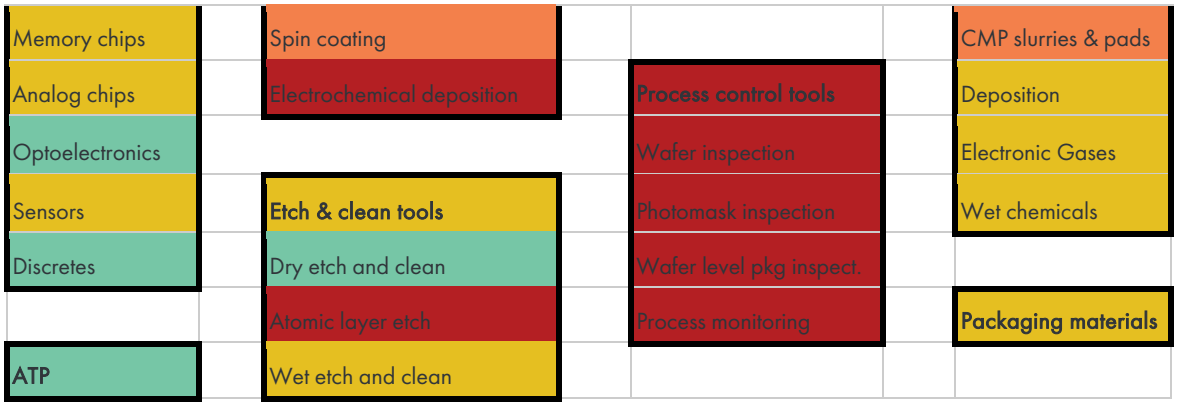
R&D	**Lithography tools**	**Assembly & pkg tools**	**CMP tools**
	EUV scanners	Assembly inspection	
Design	ArF immersion scanners	Dicing	**Ion implanters**
Logic chips	ArF dry scanners	Bonding	Low current
CPUs (logic)	KrF steppers	Packaging	High current
GPUs (logic)	i-line steppers	Integrated assembly	High voltage
FPGAs (logic)	Mask aligners		Ultra high dose
AI ASICs (logic)	E-beam lithography	**Testing tools**	
DRAM (memory)	Laser lithography	Memory	**EDA software**
NAND (memory)	Imprint lithography	System-on-a-chip	
Analog chips	Imprint lithography	Burn-in	**Core IP**
OSD	Resist processing	Linear & discrete	
		Handlers & probers	**Raw Materials**
Fab	**Deposition tools**		
Logic chips	Chemical vapor deposition	**Wafer and mask tools**	**Fab materials**
Logic foundry	Physical vapor deposition	Wafer manufacturing	Wafers
Logic IDM	Rapid thermal processing	Wafer & mask handling	Photoresists
Advanced logic	Tube-based diffusion & dep.	Wafer marking	Photomasks
Memory chips	Spin coating		CMP slurries & pads
Analog chips	Electrochemical deposition	**Process control tools**	Deposition
Optoelectronics		Wafer inspection	Electronic Gases
Sensors	**Etch & clean tools**	Photomask inspection	Wet chemicals
Discretes	Dry etch and clean	Wafer level pkg inspect.	
	Atomic layer etch	Process monitoring	**Packaging materials**
ATP	Wet etch and clean		

Note: Green: high capabilities (internationally competitive); Yellow: moderate capabilities; Orange: low capabilities; Red: minimal or no capabilities; Bolded: high-level category; Unbolded: items within and listed below high-level category. Ratings based on authors' analysis, as summarized in the following sections.

China lags behind overall, but is progressing in some segments (Table 3).[15] It excels in ATP, tools for assembly and packaging, and raw materials. It has moderate and growing capabilities in design, fabrication, CMP tools, and some etch and clean tools. China faces challenges in other segments, including most SME. Its greatest weaknesses are in EDA, core IP, some fab materials (especially photoresists), leading-edge logic fab capacity, and certain SME. These SME include lithography tools (most importantly, extreme ultraviolet scanners and argon fluoride immersion scanners), process control tools, testing tools, atomic layer etch, wafer and mask handling tools, advanced deposition tools, and some ion implanters. These weaknesses—where China has low, minimal, or no capabilities according to Table 3—are "chokepoints." They involve items necessary for advanced chip production exclusively produced by the United States and its allies.[16]

Table 3: China's competitiveness across supply chain segments

R&D	**Lithography tools**	**Assembly & pkg tools**	**CMP tools**
	EUV scanners	Assembly inspection	
Design	ArF immersion scanners	Dicing	**Ion implanters**
Logic chips	ArF dry scanners	Bonding	Low current
CPUs (logic)	KrF steppers	Packaging	High current
GPUs (logic)	i-line steppers	Integrated assembly	High voltage
FPGAs (logic)	Mask aligners		Ultra high dose
AI ASICs (logic)	E-beam lithography	**Testing tools**	
DRAM (memory)	Laser lithography	Memory	**EDA software**
NAND (memory)	Ion beam lithography	System-on-a-chip	
Analog chips	Imprint lithography	Burn-in	**Core IP**
OSD	Resist processing	Linear & discrete	
		Handlers & probers	**Raw Materials**
Fab	**Deposition tools**		
Logic chips	Chemical vapor deposition	**Wafer and mask tools**	**Fab materials**
Logic foundry	Physical vapor deposition	Wafer manufacturing	Wafers
Logic IDM	Rapid thermal processing	Wafer & mask handling	Photoresists
Advanced logic	Tube-based diffusion & dep.	Wafer marking	Photomasks



Note: Green: high capabilities (internationally competitive); Yellow: moderate capabilities; Orange: low capabilities; Red: minimal or no capabilities; Bolded: high-level category; Unbolded: items within and listed below high-level category. Ratings based on authors' analysis, as summarized in the following sections.

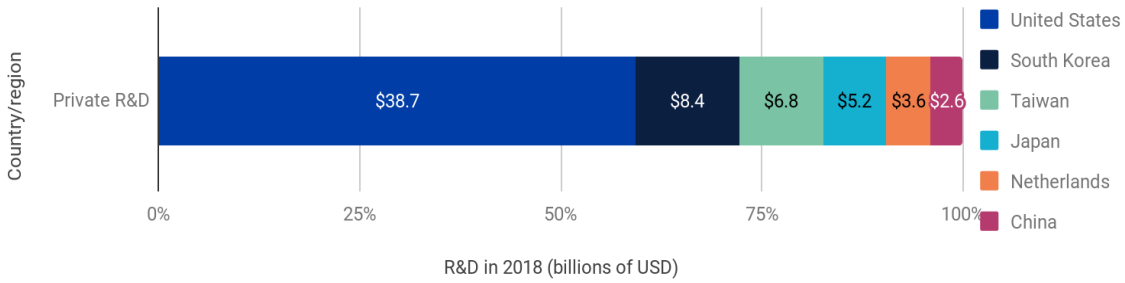
Each following section covers each country and region's national competitiveness (with extra focus on China) in each segment in detail—R&D, production (design, fabrication, and ATP), SME, EDA, core IP, and materials. (This report does not further discuss distribution and end use of semiconductors.) Although the following sections can be read in order, readers can view each section separately for an overview of that segment. Appendix B includes a glossary of terms.

Research and Development

The United States decisively leads all other countries—including China—in semiconductor R&D, which feeds into all other supply chain segments. The private sector performs most semiconductor R&D.

Figure 3 breaks down semiconductor industry R&D by firm headquarters. Globally, the semiconductor industry spent $64.6 billion on R&D in 2018 after a compound annual growth rate of 3.6 percent per year between 2013 and 2018.[17] The U.S. semiconductor industry held a commanding lead with $39.8 billion in R&D spending in 2019,[18] with five of the top 10 semiconductor firms by R&D spending in 2018.[19] By comparison, Chinese semiconductor firms spent only $2.6 billion in semiconductor R&D in 2018.[20] Countries excluded from Figure 3 account for an insignificant portion of semiconductor industry R&D. Industry R&D is mostly proprietary, but many semiconductor firms partner with competitors for R&D. One survey of 12 major semiconductor firms found nearly 200 research collaborations.[21]

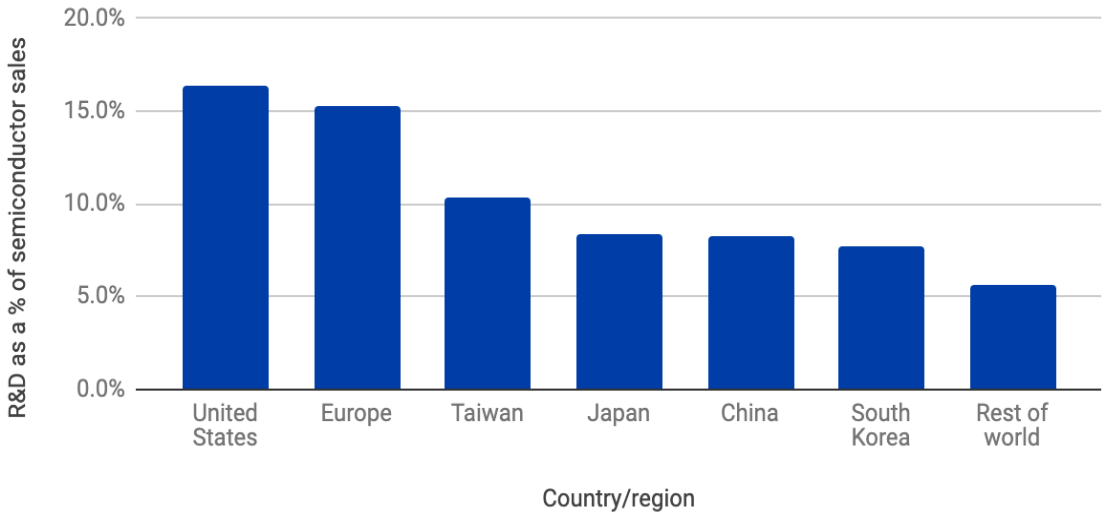
Figure 3: U.S. firms led semiconductor industry R&D in 2018



Source: SIA, SemiWiki[22]

The U.S. semiconductor industry spends the highest percentage of semiconductor sales on R&D at 16.4 percent, with China at 8.3 percent (Figure 4).

Figure 4: U.S. semiconductor firms had greater R&D intensity than counterparts in 2019



Source: SIA[23]

Governments of the United States, South Korea, Japan, Taiwan, and the Netherlands play a minor role in semiconductor R&D.[24] In 2019, the U.S. government spent $6 billion on semiconductor R&D. This amount includes $1.7 billion directly for the semiconductor sector and $4.3 billion on related technology sectors (such as engineering, computer science, mathematics, and the physical sciences).[25] Besides direct R&D funding, many governments subsidize semiconductor firms either with R&D tax breaks[26] or other funding—

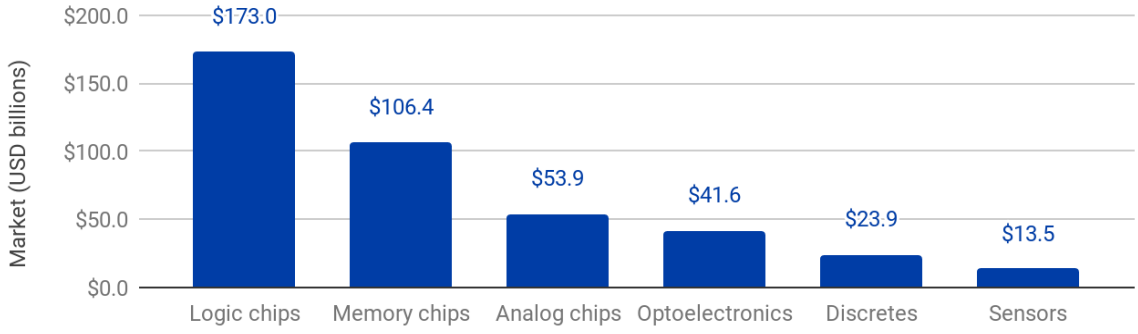
below-market financing and tax breaks for capital investment and corporate income—that firms can redirect to R&D.[27]

By comparison, the Chinese government subsidizes its semiconductor industry with about $15 billion per year.[28] These subsidies are far greater as a percentage of recipient firm revenues than government subsidies to any other countries' firms. However, China's subsidies are similar in absolute amounts to those provided by many other governments, as the globally leading semiconductor firms produce much greater revenue than do China's semiconductor firms. Moreover, China's R&D tax breaks are only a small fraction of its total subsidies—much smaller in absolute terms than U.S. R&D tax breaks.[29]

Production

The United States, South Korea, Europe, Japan, Taiwan, and China are the key countries and regions designing, fabricating, assembling, testing, and packaging semiconductors. In 2019, semiconductor production accounted for $412.3 billion in sales, with logic and memory chips taking the biggest shares (Figure 5).

Figure 5: 2019 semiconductor market

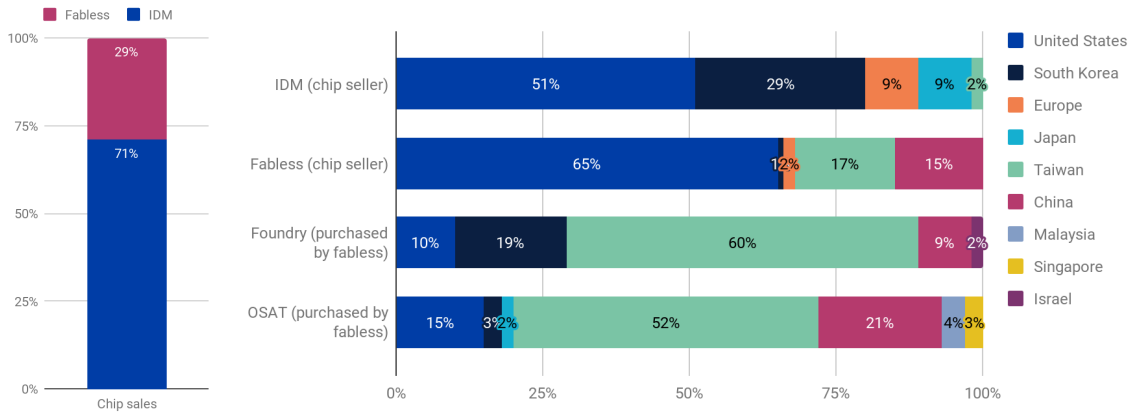


Source: WSTS[30]
Note: Logic chips include microprocessors and microcontrollers.

Semiconductors are produced under two business models.[31] In the "integrated device manufacturer" model, the same firm (an IDM) performs all three production steps. In the "fabless-foundry" model, different firms perform each step. Fabless firms design and sell the chips,[32] but buy manufacturing services from foundries and assembly, test, and packaging services from outsourced semiconductor assembly and test (OSAT) firms.[33] IDMs typically

produce memory chips, analog chips, and optoelectronics, sensors, and discretes (OSD), while logic chips are produced under both models. Figures 6 and 7 show chip sales and country shares by business model.

Figures 6 and 7: Chip sales and country shares by business model



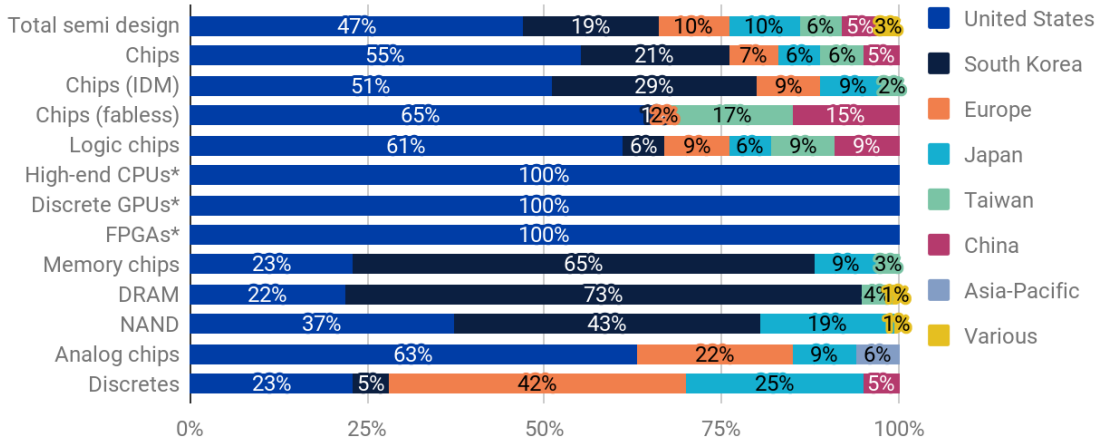
Sources: SIA, IC Insights, Yole, CSET estimates[34]

The following subsections analyze regional competitiveness for design, fabrication, and ATP. Each subsection incorporates data for both IDMs and firms operating under the fabless-foundry model.

Design

The United States, South Korea, Europe, Japan, Taiwan, and China perform almost all of the world's semiconductor design. The United States leads in logic and analog chips, South Korea in memory chips, and Europe in discretes. China designs many logic chips—though most of its chips do not compete with state-of-the-art U.S. chips—and some discretes; it is also beginning to design memory chips (Figure 8 and Table 4). (The market shares and sizes are for semiconductor sales, which include value-add from steps besides design. However, because the same firm typically designs and sells a semiconductor—even if it often outsources fabrication and ATP—these market shares correlate well with shares in design activities.) This section focuses on certain high-end logic chips and the most common memory chips.

Figure 8: 2019 design shares by type and firm headquarters



Sources: SIA, IC Insights, TrendForce, financial statements[35]
Note: China has a small share (<1%) in CPUs, GPUs, and FPGAs

Table 4: 2019 chip design market and Chinese competitiveness

Chip design type		2019 market size[36]	Top firms + Chinese firms	Chinese firm capabilities	Chinese market share
Logic chips	High-end CPUs	$56.2 billion (micro-processors)	Intel (U.S.), AMD (U.S.), Loongson (China), Zhaoxin (China), Sunway (China), Phytium (China)	**Low**: 12 nm, limited use for certain applications	<1%
	Discrete GPUs	$11.9 billion	Nvidia (U.S.), AMD (U.S.), Jingjia Micro (China)	**Low**: 28 nm, low efficiency	<1%
	FPGAs	$5.7 billion	Xilinx (U.S.), Intel (U.S.), Lattice (U.S.), Microchip (U.S.), Achronix (U.S.), Flex Logic (U.S.), Efinix (China), Gowin (China), Shenzhen Pango (China)	**Low**: 10 nm eFPGAs, 40 nm FPGAs, limited capabilities	<1%
	AI ASICs	Unavailable	Google (U.S.), Cerebras (U.S.), Intel (U.S.), Tesla (U.S.), Graphcore (U.K.), HiSilicon (China), Cambricon (China), Horizon Robotics (China), Intellifusion (China), others	**Moderate**: 7 nm, possibly competitive with leaders, but depend on foreign IP	Unavail-able

Memory chips	DRAM	$62.9 billion	Samsung (South Korea), SK Hynix (South Korea), Micron (U.S.), Nanya (Taiwan), Winbond (Taiwan), Powerchip (Taiwan), ChangXin (China)	**Moderate**: minimal capacity but expanding	<1%
	NAND flash	$40.6 billion	Samsung (South Korea), Toshiba (Japan), Western Digital (U.S.), Micron (U.S.), Intel (U.S.), SK Hynix (South Korea), YMTC (China)		

Logic chips. Logic chips perform calculations on digital data (zeroes and ones) to produce outputs. They include microprocessors (e.g. central processing units (CPUs)), microcontrollers, digital signal processors, field-programmable gate arrays (FPGAs), graphics processing units (GPUs), and other chips. The United States designs most of the world's logic chips, with South Korea, Europe, Japan, Taiwan, and China each capturing small shares. China's design sector largely consists of fabless firms designing logic chips for industries including defense, telecommunications, and finance.[37] Its fabless sector is dominated by Huawei's subsidiary HiSilicon and Tsinghua Unigroup's subsidiary Unisoc. These firms produce smartphone processors, among other chips, and are in the global top 10 fabless firms by revenue.[38] HiSilicon is in the top 10 of global semiconductor suppliers.[39] However, HiSilicon and Unisoc license core IP from U.K.-based Arm.[40] Additionally, the Chinese military is the primary consumer of Chinese logic chips, likely because export controls prevent it from accessing leading non-Chinese chips. Non-Chinese chips, especially U.S. chips, dominate China's civilian sector.[41] The following discussion focuses on four high-value logic chip categories: high-end CPUs, discrete GPUs, FPGAs, and AI ASICs.[42]

High-end central processing units. CPUs are the dominant general purpose logic chips. Two U.S. firms, Intel and AMD, have long held a duopoly over CPUs used for laptops, desktops, and servers.[43] China has several ventures, though none are competitive with U.S. firms. Loongson has developed a 12 nm CPU with homegrown IP,[44] drawing PC-maker Lenovo and Chinese supercomputer manufacturer Sugon as customers.[45] Sugon itself licensed AMD's x86 IP to develop its own CPUs, though the capabilities of these CPUs are unclear.[46] The Chinese Academy of Sciences also developed the Sunway chips powering the TaihuLight supercomputer. Moreover, Zhaoxin is developing x86 CPUs for fabrication at TSMC's 16 nm node.[47] A "node"[48] represents a technology generation; a chip at a new node (e.g., "5 nm"

released in 2020) contains approximately double the transistor density as a previous node (e.g., "7 nm" released in 2018) and is also more cost-effective.[49] Finally, Phytium produces a 28 nm CPU based on Arm's architecture for supercomputers.

Chinese CPUs have few civilian customers,[50] reflecting their lack of competitiveness on the open market. China's large businesses depend on imports for 95 percent of the CPUs they consume.[51] The country remains especially weak on CPUs with the x86 architecture, for which U.S. firms have a captive customer base.

Discrete graphics processing units. GPUs have long been used for graphics processing and in the last decade have become the most used chip for training AI algorithms.[52] The United States monopolizes the design market for GPUs, including standalone "discrete GPUs," the most powerful GPUs. Two U.S. firms, Nvidia and AMD, dominate the discrete GPU market.[53] U.S.-based Intel is also developing a discrete GPU.[54] China's only significant GPU firm is Jingjia Micro, selling largely to military customers.[55] However, its sales totaled only $36 million in 2019, and its GPUs are produced at the substandard 28 nm node.[56]

Field-programmable gate arrays. FPGAs, unlike other chips, can be reprogrammed after deployment to suit specific calculations, such as executing AI algorithms (also called "inference"). U.S. firms capture virtually the entire FPGA design market.[57] China's three FPGA-makers largely manufacture at very old nodes, between 40 and 55 nm.[58] An exception is Efinix's development of a 10 nm "eFPGA," a stripped-down version of an FPGA whose designs can be incorporated into other chips.[59] On balance, China's FPGAs are not competitive with U.S. counterparts.

Application-specific integrated circuits for artificial intelligence. AI ASICs often achieve greater speed and efficiency for artificial intelligence than GPUs and FPGAs, but are usable only for specific AI algorithms.[60] From 2017 to 2019, most of the venture capital investment in fabless firms went to AI chip design startups.[61] More firms are developing these chips and China has advanced the most, as ASICs can be easier to design than CPUs, GPUs, and FPGAs.[62] Still, few highly specialized ASICs have been widely commercialized, as their markets are often too small for recouping fixed development costs. China does best with AI inference ASICs, though its firms are also developing AI training ASICs. A notable example of the latter is Huawei's Ascend 910, fabricated at TSMC's 7 nm node and competitive

with leading firms.[63] However, Huawei's chip designs license foreign IP from the U.K.-based, Japanese-owned ARM.

Memory chips. Memory chips store the digital data on which logic devices perform calculations. DRAM provides "volatile" storage of data while a computer operates, but loses it when the computer powers down. By contrast, NAND flash memory is "non-volatile," storing memory permanently. South Korea, the United States, and Taiwan control the market for DRAM design, while South Korea, the United States, and Japan do for NAND flash memory. China is attempting to produce DRAM and NAND chips as well. These chips comprise 98 percent of the memory chip market.[64] Although Chinese firms currently account for only a small amount of memory chip production, ChangXin is developing capacity to produce 3 percent of the world's DRAM output and YMTC to produce 5 percent of the world's NAND flash memory output.[65] Memory chips are more commoditized and easier to produce than logic chips, and producers mostly compete on price—a strategy at which Chinese firms excel. A larger barrier is access to patent licenses from industry leaders,[66] though Chinese memory chip suppliers are acquiring them.[67] Therefore, memory chip design is unlikely to remain a major chokepoint for China.[68]

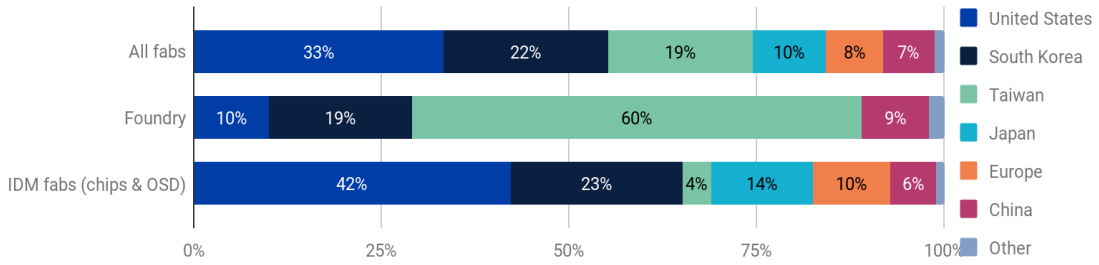
Fabrication

Firms headquartered in the United States, Taiwan, South Korea, Japan, and China control the vast majority of the world's fab market share (Figure 9) and fab capacity (Figure 10 and Table 5)—most of which is also physically located in these countries (Figure 11). There are two business models for fabs: (1) fabs owned by IDMs, which manufacture chips based on their own designs; and (2) foundries, i.e., fabs operating independently and manufacturing chips for third-party customers. However, although China's shares look strong, much of that capacity is aspirational (suffering from low yields and utilization) and at older nodes. Many of these fabs stay online with the help of state support, receiving subsidies far greater as a percentage of revenue than any leading fabs.[69] Foreign chipmakers operate the most advanced and reliable fabs in China and generate more revenue than the country's chipmakers.[70]

Advanced logic capacity represents China's greatest weakness in fabs, though it is attempting to build such capacity. Additionally, logic chips (e.g. CPUs, GPUs, FPGAs, and AI ASICs) are especially critical for applications

relevant to national and international security. The remainder of this section therefore focuses on logic fab capacity.

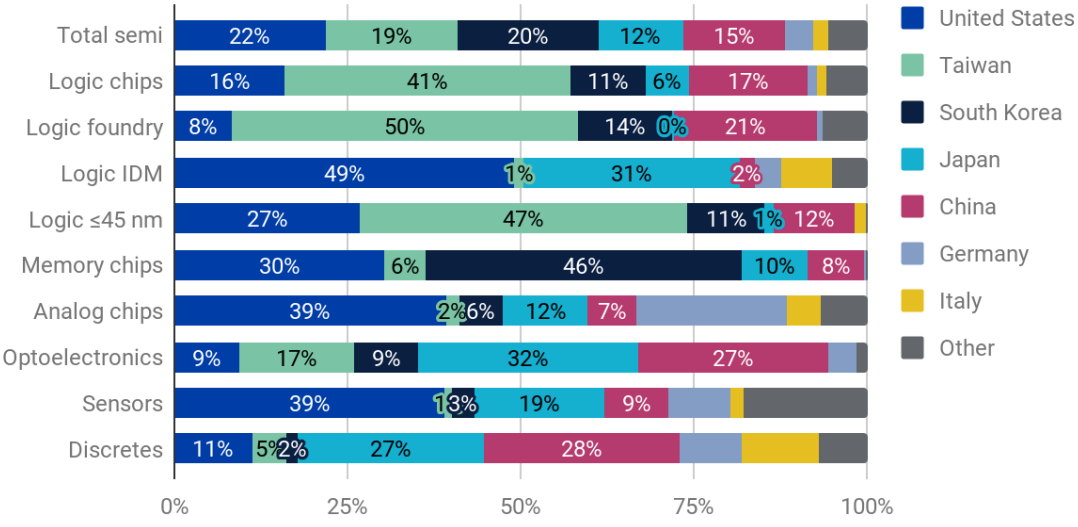
Figure 9: 2019 market share by fab type and firm headquarters



Sources: CSET calculations, IC Insights, SIA, SEMI, WSTS[71]

Figure 10 shows fab capacity shares by firm headquarters for several categories. These categories include capacity for all semiconductors, logic chips (including capacity held by both foundries and IDMs), memory chips, analog chips, optoelectronics, sensors, and discretes. A more detailed breakdown is provided for logic chips. Specifically, Figure 10 includes logic chip capacity respectively held by IDMs and foundries, as well as logic chip capacity (held by both foundries and IDMs) at or below the 45 nm node.

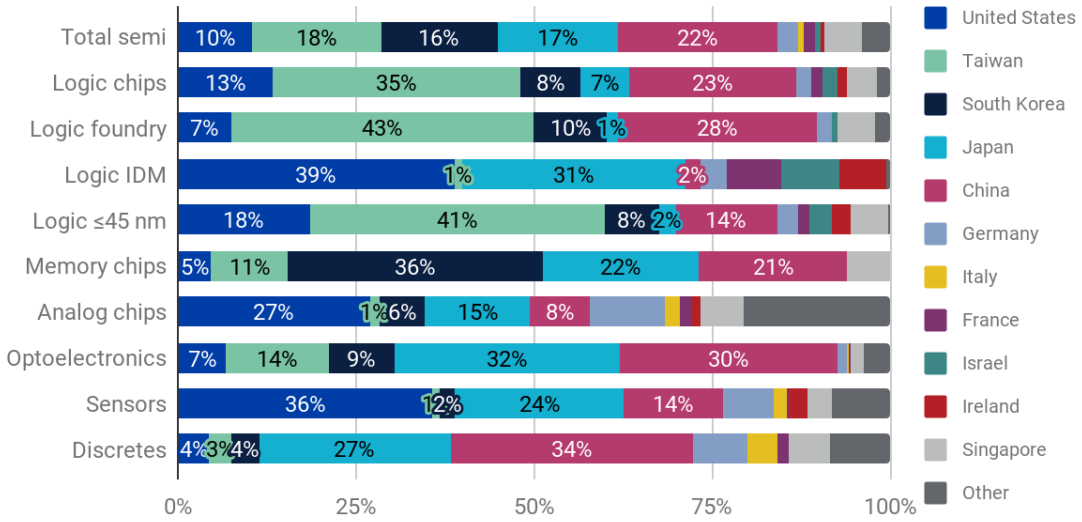
Figure 10: 2020 wafer fab capacity by fab type and firm headquarters



Source: "World Fab Forecast," SEMI, November 2020 edition[72]

Figure 11 shows fab capacity shares by fab location, broken down according to the same categories as in Figure 10.

Figure 11: 2020 wafer fab capacity by fab type and fab location



Source: "World Fab Forecast," SEMI, November 2020 edition

Table 5: 2019 fab market and Chinese competitiveness

Fab type[73]		**Fab capacity share**	**Top firms + Chinese firms**	**Chinese firm capabilities**	**Chinese HQ fab share**
Foundry	Logic chips	28%	TSMC (Taiwan), Samsung (South Korea), Global Foundries (U.S.), SMIC (China), UMC (Taiwan), Powerchip (Taiwan), Hua Hong (China), others	**Moderate**: small amount of low-yield 14 nm capacity	21%
IDM		6%	Intel (U.S.), Renesas (Japan), STMicroelectronics (Switzerland), Microchip (U.S.), NXP (U.S./Netherlands), Toshiba (Japan), others	**Low**: Minimal capabilities	2%
	Memory chips[74]	32%	SK Hynix (South Korea), Samsung (South Korea), Micron (U.S.), Toshiba	**Moderate**: capacity developing but largely aspirational	8%

IDM, cont'd			(Japan), Western Digital (U.S.), Intel (U.S.), YMTC (China), ChangXin (China), others		
	Analog chips	7%	Texas Instruments (U.S.), ON (U.S.), SiEn (China), ASMC (China), Bosch (Germany), STMicroelectronics (Switzerland), TowerJazz (Japan), others	Moderate	7%
	Opto-elec-tronics	7%	Sony (Japan), Nichia (Japan), Samsung (South Korea), Osram (Germany), HC SemiTek (China), Epistar (Taiwan), Sanan (China), Aucksun (China), Changelight (China), others	High	27%
	Sensors	2%	Qorvo (U.S.), Broadcom (U.S.), Seagate (U.S.), Texas Instruments (U.S.), OmniVision (China), SMIC (China), others	Moderate	9%
	Discrete	12%	Infineon (Germany), STMicroelectronics (Switzerland), Hangzhou (China), ON (U.S.), Mitsubishi (Japan), AOS (U.S.), CR (China), Yangzhou (China), others	High	28%

Firms headquartered in the United States, Taiwan, South Korea, Japan, and China control most of the world's logic capacity—and also keep most of it within their borders. Foundries control more than 80 percent of the world's logic fab capacity (Table 5). Three firms – headquartered in the United States (Intel), Taiwan (TSMC), and South Korea (Samsung) – control virtually all of the world's advanced logic fab capacity (≤10 nm), though U.S.-based Intel is building such capacity in Israel and Ireland.[75]

Winner-take-all dynamics pose challenges to follow-on competitors in the logic foundry industry. Market leader TSMC has 54 percent of the world's logic foundry market share and an even larger market share for leading-edge logic foundries.[76] Now it produces state-of-the-art 5 nm node chips and is

rapidly increasing revenue per wafer while other chipmakers operating foundries are seeing declines—including U.S.-based GlobalFoundries, Taiwan-based UMC, and China's most advanced chipmaker, SMIC.[77] Samsung is also introducing 5 nm logic foundry capacity, while Intel is fabricating 10 nm logic chips with specifications competitive with TSMC's 7 nm node chips.[78] The United States has strong capacity, though its most advanced logic foundries, held by GlobalFoundries, are at 12 nm. U.S.-based IDM Intel still plans to introduce 7 nm node chips with specifications competitive with TSMC's 5 nm node chips, but is falling behind, with plans to introduce them by 2022 or early 2023.[79]

Because of minimal and low quality leading-edge capacity, Chinese foundries face difficulty attracting foreign fabless customers.[80] SMIC has reached 14 nm, but at a capacity of only 6,000 wafers per month (0.2 percent of the world's ≤16 nm logic fab capacity), with plans to increase to 35,000 (1 percent).[81] Chinese chipmaker Hua Hong is also attempting to develop 14 nm capacity.[82] To compete with TSMC, Chinese foundries must overcome know-how deficits and rely on subsidies to invest in leading-edge capacity—whose costs rise quickly from one node to the next.[83] If applied, future U.S., Japanese, and Dutch export controls on SME and materials could prevent Chinese foundries from building advanced capacity. The current Dutch ban on exports of EUV scanners to China already prevents it from building capacity more advanced than 7 nm.[84]

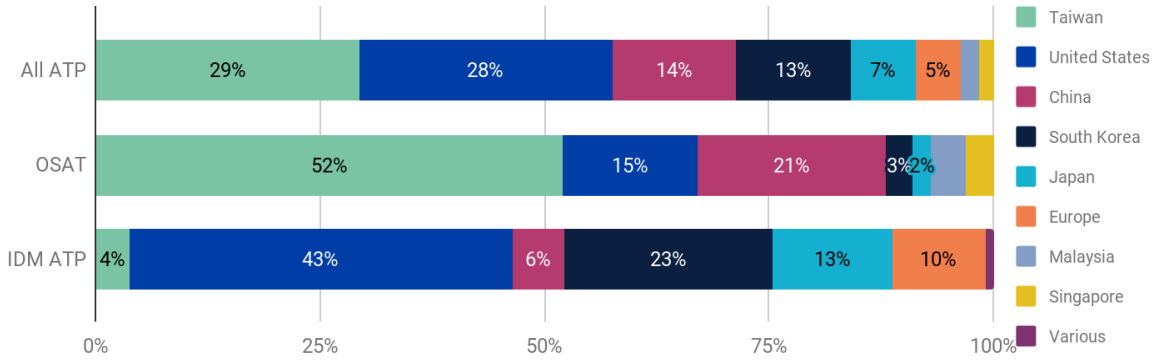
Assembly, Testing, and Packaging

ATP occurs under two business models: (1) as in-house ATP services performed by integrated device manufacturers (IDMs) and foundries after fabrication; and (2) by outsourced semiconductor assembly and test (OSAT) firms, which perform ATP for third-party customers. ATP is labor-intensive and lower value than design and fabrication, and does not develop skills in these two segments. Therefore, firms historically set up ATP facilities in developing countries.[85]

Firms headquartered in Taiwan, the United States, China, and South Korea are the main providers of ATP services (Figure 12 and Table 6). China benefited from offshoring, developing a strong ATP industry—its OSAT industry is the world's second largest after Taiwan. Additionally, non-Chinese IDMs keep many ATP facilities in China. Although the top three ATP firms in China are Chinese OSATs, the rest of the top 10 are non-Chinese IDMs (six

American).[86] Therefore, ATP is arguably a supply chain vulnerability for the United States. Overall, 22 percent of the world's ATP facilities are in China.[87] Although ATP was historically low value, packaging has increasingly become a bottleneck on chip performance.[88] Densities of transistors in logic and memory units in chips have continued to increase exponentially, but the density of interconnects between logic and memory—governed by packaging—have increased at a much slower rate, leading to communication bottlenecks between chips.[89] Additionally, the rates of increases in density of logic and memory may slow,[90] providing comparatively more innovation opportunities for advanced packaging.[91]

Figure 12: Country market shares by firm headquarters



Source: Yole, SIA, SEMI, IC Insights, WSTS, CSET calculations[92]

Table 6: ATP market and Chinese competitiveness

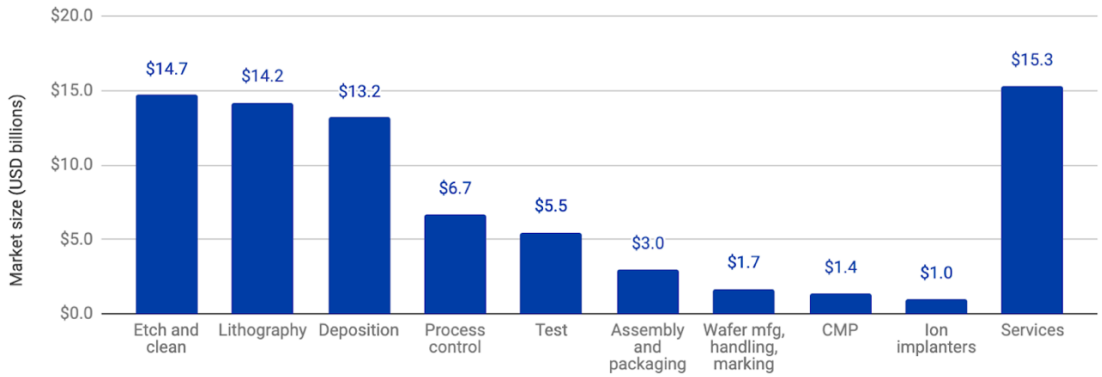
Sector	2019 market size	Top firms + Chinese firms	Chinese firm capabilities	2018 Chinese market share
Outsourced semiconductor assembly and test	$28 billion	ASE (Taiwan), Amkor (U.S.), JCET (China), Powertech (Taiwan), TongFu (China), Tianshui (China), UTAC (Singapore), others	**High**	21%
In-house ATP (by foundries and IDMs)[93]	$25 billion	Intel (U.S.), Samsung (U.S.), S.K. Hynix (South Korea), Micron (U.S.), TSMC (Taiwan), others	**Minimal**	6%

Semiconductor Manufacturing Equipment

The United States, Japan, and the Netherlands dominate the production of SME, the most severe chokepoint in China's chip supply chains. There are dozens of categories of SME (Figures 13 and 14 present 2019 SME market sizes and country shares by segment).[94] "Services" include support services provided by SME firms to help with setup, troubleshooting, and repair of any SME. Most SME is used for making chips or inputs to them. These tools include those for wafer manufacturing, wafer and photomask handling, wafer marking, ion implantation, lithography, deposition, etch, clean, chemical mechanical planarization, and process control. Specialized tools are also used for assembly, testing, and packaging.

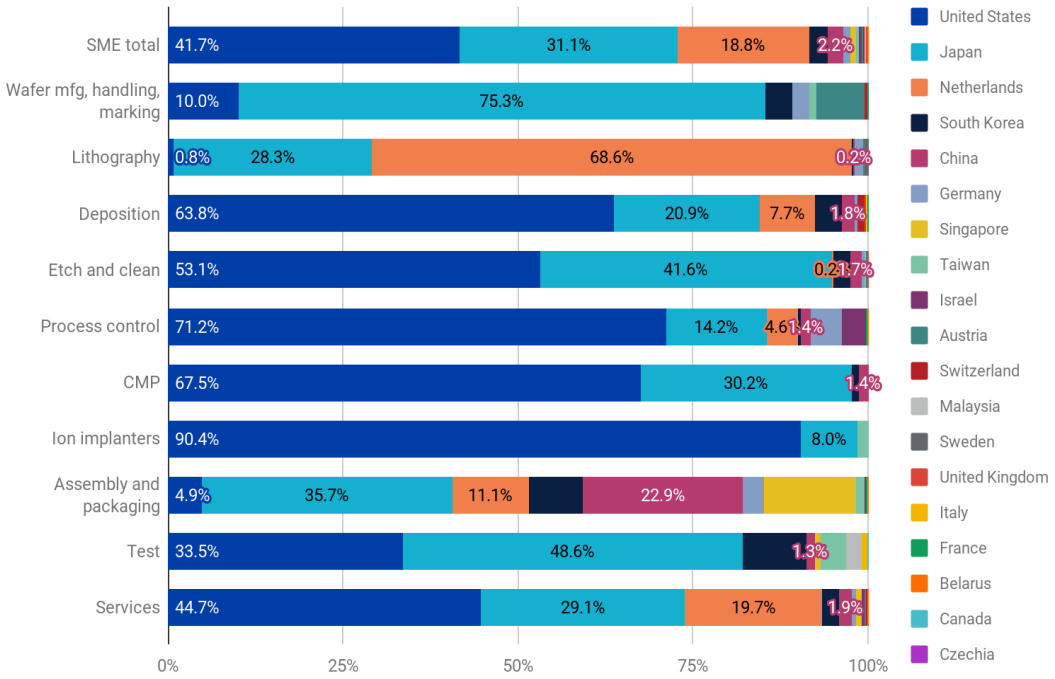
China has little to no market share in all major segments, except for assembly and packaging tools.[95] China's most critical chokepoint is in lithography tools—especially extreme ultraviolet (EUV) photolithography and deep ultraviolet (DUV) photolithography, but also imprint lithography, e-beam lithography, laser lithography, resist processing equipment, and photomask inspection and repair tools. Other tools are also chokepoints, especially those for advanced ion implantation, atomic layer etching, advanced chemical vapor deposition, wafer and mask handling, wafer and photomask inspection, and testing advanced logic chips. Companion CSET policy briefs titled "Securing Semiconductor Supply Chains"[96] and "China's Progress in Semiconductor Manufacturing Equipment"[97] offer recommendations on export controls and other policies affecting SME that could slow China's development in indigenizing both SME and leading-edge chipmaking capacity.

Figure 13: 2019 SME market by SME type



Source: VLSI Research

Figure 14: 2019 SME country shares by firm headquarters

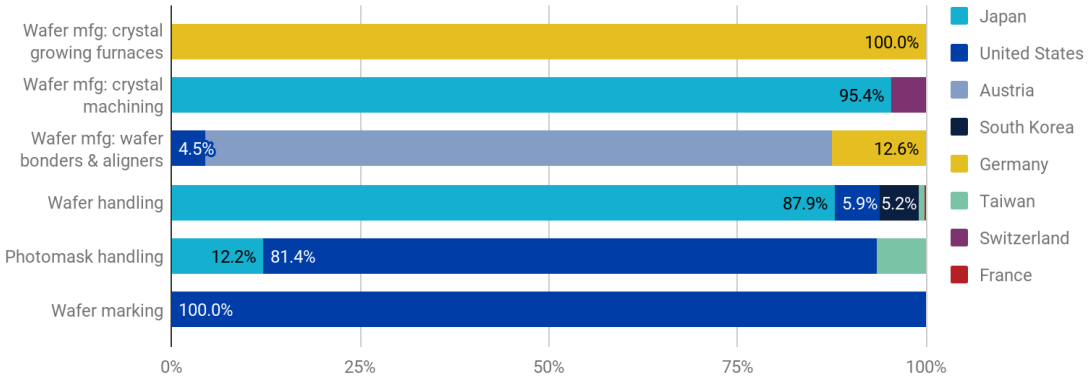


Source: VLSI Research

Wafer Manufacturing, Wafer Marking, and Handling

Japan, the United States, and Austria are key producers of wafer manufacturing, handling, and marking equipment. (Figure 15 and Table 7). China's producers have minimal capabilities and market share. Given their higher value, wafer manufacturing equipment and handling systems are chokepoints for China.

Figure 15: 2019 wafer manufacturing, wafer marking, and handling country shares by firm headquarters



Source: VLSI Research

Table 7: 2019 wafer manufacturing, wafer marking, and handling market and Chinese competitiveness

Equipment		2019 market size	Top firms + Chinese firms	Chinese firm capabilities	Chinese market share
Wafer mfg.	Crystal growing furnaces	$21 million	PVA TePla (Germany), JSG (China)	Low	<1%
	Crystal machining	$110 million	Accretech (Japan), Okamoto (Japan), Disco (Japan), Meyer Burger (Switzerland), Toyo (Japan), JSG (China), Lanzhou Rapid Equipment Manufacturing (China), Beijing JingYi Century Automatic Equipment (China)		
	Wafer bonders & aligners	$140 million	EV Group (Austria), SUSS MicroTec (Germany), Neutronix (U.S.), SMEE (China)		
Handling	Wafer handling	$1.3 billion	Daifuku (Japan), Rorze (Japan), Semes (South Korea), Muratec (Japan), Gudeng (Taiwan), RECIF (France), SMEE (China)		

	Photomask handling	$99 million	Brooks (U.S.), Daifuku (Japan), Gudeng (Taiwan), RECIF (France)		0%
Wafer marking systems		$500 thousand	ESI (U.S.)		

Crystal growing furnaces and machining tools are necessary to produce all wafers—thin, disc-shaped materials fabs used to produce chips.[98] These tools have relatively lower value and complexity relative to other SME. Japan, Germany, and Switzerland are the main producers, while China has a few insignificant producers and relies on imports.[99]

Wafer bonders and aligners join silicon wafers, often after chips are fabricated in the wafers. Austria, Germany, and the United States produce this equipment, while China does not. Shanghai Micro Electronics Equipment (SMEE) markets these tools, but has minimal sales and capabilities.[100]

Wafer and photomask handlers store and transport wafers and photomasks in a fab. Photomasks are transparent plates containing a circuit pattern that photolithography tools pass light through to transfer the pattern to the chip. Japan, South Korea, Taiwan, and France produce wafer and photomask handlers, which China does not produce. It is unclear whether this is an important chokepoint for China, as the tools are not as complex as other SME; thus, China may eventually produce them.

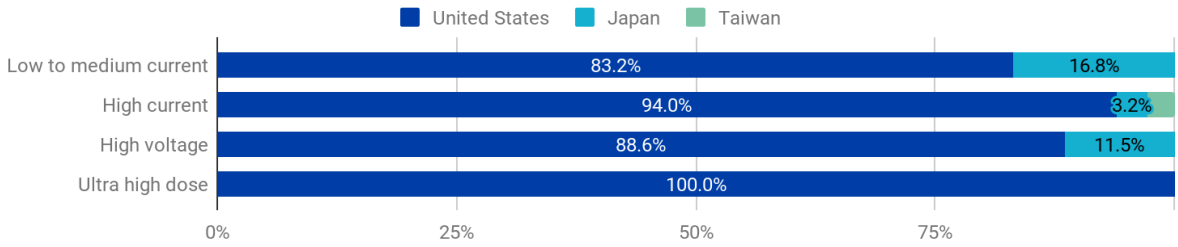
Wafer marking systems mark wafers, or chips manufactured in wafers, with identifiers using a laser. The United States solely produces this equipment. However, other countries, including China, could readily develop this technology given its low complexity and expense.

Ion Implanters

Ion implanters embed dopants into silicon wafers to give different parts of the wafer different levels of semiconductivity to make functional transistors in chips.[101] Four categories are needed for different use-cases.[102] Low-to-medium-current ion implanters and high-current ion implanters are most commonly used, with high-current ion implanters capable of greater throughput. High-voltage ion implanters can implant ions deeply into silicon. Ultra-high-dose doping implanters can achieve greater dopant density than the other tools.

The United States is the dominant producer of ion implanters, with Japan and Taiwan rounding out most of global market share (Figure 16 and Table 8). China produces a small amount of less-advanced ion implanters for specialized purposes, but not ion implanters for leading-edge logic chips, making it a moderate chokepoint. China has two minor producers. State-owned defense conglomerate China Electronics Technology Group produces a variety of ion implanters for discrete semiconductors and chips based on silicon carbide and gallium arsenide[103] with 28 nm capabilities[104] and estimated sales of $15 million per year.[105] Kingstone Semiconductor produces high-current ion implanters for photovoltaics.[106]

Figure 16: 2019 ion implanters country shares by firm headquarters



Source: VLSI Research

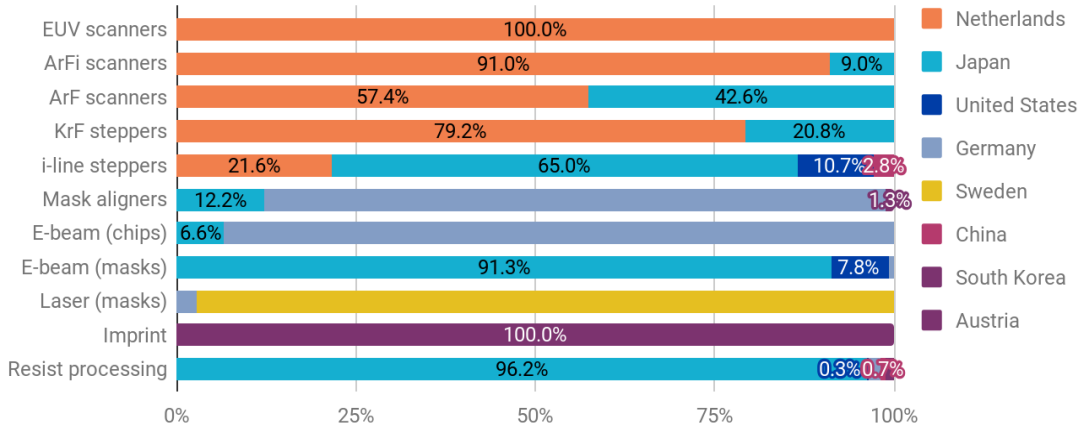
Table 8: 2019 ion implanters market and Chinese competitiveness

Equipment	2019 market size	Top firms + Chinese firms	Chinese firm capabilities	Chinese market share
Low to Medium Current Implanters	$0.24 billion	Applied Materials (U.S.), Nissin Ion (U.S.), SMIT (Japan), Axcelis (U.S.), CETC (China)	**Low:** ≥28 nm, used for discretes, silicon carbide chips, gallium arsenide chips, and photovoltaics	<2%
High Current Ion Implanters	$0.58 billion	Applied Materials, (U.S.), Axcelis (U.S.), SMIT (Japan), Hermes-Epitek (Taiwan), CETC (China), Kingstone Semiconductor (China)		
High Voltage Ion Implanters	$0.22 billion	Axcelis (U.S.), Applied Materials (U.S.), SMIT (Japan), CETC (China)		
Ultra High Dose Doping Implanters	$8 million	Applied Materials (U.S.)	**None**	0%

Lithography

The Netherlands, Japan, and a small number of other countries are the dominant producers of lithography equipment, critical for the production of chips and photomasks (Figure 17 and Table 9). China cannot produce any advanced lithography equipment. Most importantly, the Netherlands and Japan are exclusive providers of advanced photolithography equipment—especially extreme ultraviolet (EUV) scanners and secondarily argon fluoride (ArF) immersion scanners—necessary for mass-production of advanced chips, representing China's top chokepoint.

Figure 17: 2019 lithography country shares by firm headquarters



Source: VLSI Research

Table 9: 2019 lithography market and Chinese competitiveness

Equipment		2019 market size	Top firms + Chinese firms	Chinese firm capabilities	Chinese market share
Photo-lithography	EUV scanners	$3.1 billion	ASML (Netherlands)	**None**	0%
	ArFi scanners	$5.8 billion	ASML (Netherlands), Nikon (Japan)	**None**: but developing 28 nm tool	
	ArF scanners	$0.78 billion	ASML (Netherlands), Nikon (Japan), SMEE (China)	**Moderate**: 90 nm tool, but limited	

				capabilities for mass chip fab	
	KrF steppers	$0.96 billion	ASML (Netherlands), Canon (Japan), Nikon (Japan), SMEE (China)	**Moderate:** 110 nm tool, but limited capabilities for mass chip fab	
	i-line steppers	$0.69 billion	Canon (Japan), ASML (Netherlands), Nikon (Japan), Veeco (U.S.), SMEE (China), Institute of Optoelectronic Technology (China), others	**Moderate:** 280 nm tool used largely for packaging, not chip fab	2.8%
	Mask aligners	$0.12 billion	SUSS MicroTec (Germany), Toray (Japan), USHIO (Japan), EV Group (Austria)	**None**	0%
Electron-Beam lithography	Chip-making	$20 million	Vistec (Germany), JEOL (Japan)		
	Mask-making	$0.49 billion	NuFlare (Japan), JEOL (Japan), Applied Materials (U.S.), Vistec (Germany)		
Laser lithography		$85 million	Mycronic (Sweden), Heidelberg Instruments (Germany)		
Ion beam lithography		Minimal [107]	Thermo Fisher (U.S.), Hitachi (Japan), Zeiss (Germany), Tescan (Czechia), JEOL (Japan), HORIBA (Japan), Eurofins (Luxembourg), A&D (Japan), Raith (Germany), FOCUS (Germany), others		
Imprint lithography		$24 million	EV Group (Austria), Canon (Japan), Nanonex (U.S.), SUSS MicroTec (Germany), Obducat (Sweden)		
Resist processing (tracks)		$2.1 billion	Tokyo Electron (Japan), Screen (Japan), SUSS MicroTec (Germany), SEMES (South Korea), Kingsemi (China), Brewer Science (U.S.), Rite Track (U.S.)	**Low:** i-line, KrF, and ArF, not currently ArFi & EUV	0.7%

Table 10 summarizes the capabilities of lithography tools. (It excludes resist processing equipment, which complements lithography equipment.) Photolithography tools are used in high-volume chip production, and currently include six grades from most to least advanced by supported nodes: EUV, deep ultraviolet (DUV)—which includes ArF immersion (also called wet ArF or ArFi), ArF (also called dry ArF), and krypton fluoride (KrF)—i-line, and mask aligners. An older grade, g-line, is no longer used. Other types of lithography equipment are for specific, lower-volume chips or photomasks (e-beam and laser) or are emerging areas of development for future mass chip production (imprint).

Table 10: Lithography types

<table>
<tr><td rowspan="4">Type</td><td colspan="7">Photolithography</td><td rowspan="4">Imprint litho-graphy</td><td rowspan="4">Electron-beam lithography</td><td rowspan="4">Laser litho-graphy</td><td rowspan="4">Ion beam litho-graphy</td></tr>
<tr><td rowspan="3">Mask aligner</td><td colspan="2">Stepper</td><td colspan="3">Scanner</td></tr>
<tr><td rowspan="2">g-line</td><td rowspan="2">i-line</td><td colspan="3">DUV</td><td rowspan="2">EUV</td></tr>
<tr><td>KrF</td><td>ArF</td><td>ArFi</td></tr>
<tr><td>Source (nm)</td><td>Various</td><td>436</td><td>365</td><td>248</td><td colspan="2">193</td><td>13.5</td></tr>
<tr><td>Node (nm)[108]</td><td>Trailing</td><td>≥1,000</td><td>≥350</td><td>≥150</td><td>≥65</td><td>≥7</td><td>≥5</td><td colspan="3">Competitive with advanced scanners</td></tr>
<tr><td>Uses mask</td><td colspan="8">Yes</td><td colspan="3">No (typically direct-write)</td></tr>
<tr><td>High volume</td><td colspan="8">Yes</td><td>Future?</td><td colspan="2">No</td></tr>
<tr><td>Key use case</td><td colspan="9">Chips</td><td>Photomasks and chips</td><td>Photomasks</td></tr>
</table>

Photolithography: scanners and steppers. The Netherlands and Japan dominate the production of scanners and steppers—the photolithography equipment needed to mass-produce chips. The United States and China have small market shares in less advanced steppers. One Dutch firm, ASML, exclusively produces EUV scanners, the most advanced photolithography equipment. ASML and Japan-based Nikon exclusively produce ArF immersion scanners, the next most advanced. Scanners and steppers produce

light that passes through a photomask to transfer previously created circuit patterns in the photomask onto multiple wafers.[109]

This equipment is China's top chokepoint due to its technical complexity and expense. First, scanners are the only tools combining high precision (by producing light with small wavelengths) and high throughput (by using photomasks, as will be described in the following "Maskless lithography" subsection). EUV scanners are necessary for mass-producing 5 nm node chips, while EUV and ArF immersion scanners together are the only lithography tools capable of mass-producing chips in the 28 to 7 nm node range, with ArF immersion in predominant use for even 45 nm (Table 10). Second, EUV and ArF immersion scanners are the most expensive[110] tools used in chip fabrication, taking an increasingly large share of chip fabrication costs.[111] With "100,000 parts, 3,000 cables, 40,000 bolts and 2 kilometers of hosing," an EUV scanner is more complex than any SME and a typical car, which has tens of thousands of parts.[112] These trends are also making markets for photolithography more consolidated[113] and profitable[114] than for other high-value SME. Third, they require the greatest precision, being responsible for drawing the nanoscale circuit patterns in chips. Fourth, EUV scanners simplify and reduce the need for non-lithography fabrication steps,[115] further increasing photolithography's importance relative to other SME.[116] For these reasons, improvements in photolithography also constrain Moore's Law improvements in transistor density—spurring the leading chipmakers Intel, Samsung, and TSMC to preferentially invest in ASML to support its EUV R&D.[117]

China is developing scanners and steppers. Shanghai Micro Electronics Equipment (SMEE) has purportedly developed a 90 nm ArF tool and plans to introduce a 28 nm ArF immersion tool by 2021 or 2022.[118] Still, even if these reports are true and the tools work, building a mass-production-ready tool with low cost, low manufacturing error rates, and high throughput can take years after initial prototyping.[119] Even Chinese fabs are not yet using SMEE's 90 nm steppers for mass chip production. Instead, SMEE's photolithography tools are used for the less difficult step of chip packaging (not fabrication),[120] and mostly not for advanced packaging techniques.[121] Besides SMEE, in 2018, China's state media reported that the Institute of Optoelectronic Technology in the Chinese Academy of Sciences developed an experimental photolithography tool with a 365 nm i-line light source that achieves 22 nm resolution and in the future could achieve 10 nm.[122] This resolution capability is inconsistent with known i-line technology, so the report is likely not credible.

Finally, some Chinese research institutes are attempting to develop components for EUV, but it is unclear whether they will succeed.[123]

Photolithography: mask aligners. Only Germany, Japan, and Austria produce mask aligners. Mask aligners are an alternative form of photolithography where—unlike scanners and steppers—the wafer and photomask remain in fixed relative position, either in direct physical contact or in close proximity. However, this form of photolithography does not achieve small feature sizes competitive with scanners and steppers.[124] Therefore, mask aligners only have special use-cases, are low value, and lack strategic importance.

Maskless lithography: electron-beam, laser, and ion beam. Only Japan, Germany, the United States, and Sweden produce electron-beam (e-beam) and laser lithography tools, representing a critical chokepoint for China for photomask production. These countries and others also produce ion beam lithography tools, which could be used for photomask production (but rarely are). Laser lithography tools (like photolithography tools) draw patterns with light beams. By contrast, e-beam and ion beam lithography tools draw patterns with electrons and ions, respectively.[125] These tools can achieve similar resolution as advanced photolithography tools.[126] The key difference is that e-beam, laser, and ion beam lithography tools do not use masks. The advantage is that these tools can quickly and cheaply make new patterns without a new mask. The disadvantage is that drawing patterns is slow without a mask. Therefore, e-beam, laser, and ion beam lithography tools can cost-effectively produce low-volume items like photomasks used with photolithography tools. (Far fewer photomasks are needed than chips, because a small number of photomasks are used to produce a large number of chips during photolithography.) But these tools are ill-suited to mass chip production given their low throughput. E-beam tools are the dominant tools for photomask production, with laser lithography tools a distant second, and ion beam lithography tools rarely used. Besides photomasks, about 4 percent of the e-beam tool market is used for low-volume chip production (Table 9), while laser lithography tools are not normally used for chip production.

Imprint lithography. Today, Austria is the main seller for semiconductor applications, while Japan, the United States, and Germany are either selling or developing for various other applications. Imprint lithography is a potentially important chokepoint for China, as it could compete with photolithography in mass chip production. Imprint lithography can achieve

leading-edge, nanoscale resolutions—and therefore is often called nanoimprint lithography. It also uses a template, which plays a similar role as a photomask in photolithography. The template contains a pattern that is transferred to a wafer. Given its use of a template, imprint lithography can theoretically achieve high-volume production. However, it has low yields and produces too many defects to compete with photolithography.[127] The main firm selling it today for semiconductors, EV Group, has small sales geared toward narrow use-cases. Toshiba plans to use Canon's nanoimprint technology to make 3D NAND memory chips.[128] SUSS MicroTec, Nanonex, and Obducat are also producers.

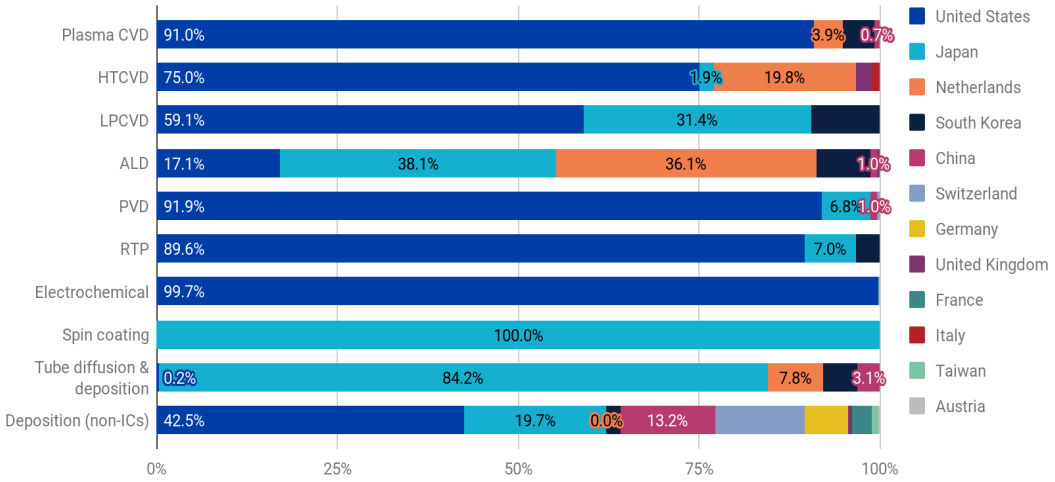
Resist processing. Japan is a dominant producer of resist processing tools (also called "tracks"). Germany, South Korea, the United States, and China each have small market shares. However, only Japan is the key producer of the most advanced tracks for EUV and ArF immersion photolithography.[129] Photoresists are chemicals deposited on a wafer that, when exposed to patterned light that has passed through a photomask, selectively dissolve to form the circuit pattern. Etching is then performed in places where the photoresist has dissolved to transfer the circuit pattern permanently onto the wafer. Resist processing tools coat photoresists on wafers (typically by spin-coating, which spins the wafer to spread deposited photoresist), develop them (dissolve portions hit by light), and bake them (harden undissolved photoresist to prepare for etching). China's only firm, Kingsemi, produces tracks for ArF, KrF, and i-line photolithography, and claims it will develop EUV and ArF immersion tracks by 2022.[130] However, Kingsemi also purportedly supports ≥28 nm nodes, which is normally in the ArF immersion range.[131] Because China does not currently produce tracks for EUV or more advanced ArF immersion photolithography, these tracks are currently a chokepoint for China.

Deposition

The United States, Japan, the Netherlands, and South Korea are leading providers of deposition tools, while China has a small but growing share in certain deposition market subsectors (Figure 18 and Table 11). Still, China has chokepoints across the board, such as for rapid thermal processing tools. Deposition tools are used to deposit thin films of materials on a silicon wafer. After lithography and etching, these films become different chip layers, including for transistors, interconnects (wires), and other elements. The vast majority of deposition tools are used for chip production, so the technology

categorizations in this section are all specific to chip production, except for a final catch-all category for the non-chip deposition market.

Figure 18: 2019 deposition country shares by firm headquarters



Source: VLSI Research

Table 11: 2019 deposition market and Chinese competitiveness

Equipment		2019 market size	Top firms + Chinese firms	Chinese firm capabilities	Chinese market share
Chemical vapor deposition	Plasma CVD	$3.5 billion	Applied Materials (U.S.), Lam Research (U.S.), ASM Int. (Netherlands), Piotech (China), SKY Technology Development (China), others	**Moderate**: dielectric for 5 nm	0.7%
	Low pressure CVD	$1.4 billion	Lam Research (U.S.), Applied Materials (U.S.), Tokyo Electron (Japan), NAURA (China), others	**Moderate**: several key chip materials	<1%
	High temp. CVD	$0.97 billion	Applied Materials (U.S.), ASM Int. (Netherlands), others	**None**	0%
	Atomic layer deposi-tion	$1.6 billion	ASM Int. (Netherlands), Tokyo Electron (Japan), Kokusai (Japan), Lam Research (U.S.),	**Low**: many materials ≥14 nm & some materials <14 nm	1.0%

			Piotech (China), NAURA (China), others		
Physical vapor deposition		$2.4 billion	Applied Materials (U.S.), ULVAC (Japan), NAURA (China), KLA (U.S.), SKY Technology Development (China)	**Low**: many materials ≥28 nm	1.0%
Rapid thermal processing		$0.56 billion	Applied Materials (U.S.), Mattson Tech (U.S.), Screen (Japan), AP Systems (South Korea), Veeco (U.S.)	**None**	0%
Tube-based diffusion and deposition		$1.5 billion	Tokyo Electron (Japan), Kokusai, (Japan), ASM Int. (Netherlands), NAURA (China), others	**Low**: ≥28 nm for diffusion, none for deposition	3.1%
Spin coating		$46 million	Screen (Japan)	**Low**: mostly for coating photoresists	0%
Electrochemical deposition		$0.29 billion	Lam Research (U.S.), Applied Materials (U.S.), Grand Plastic (Taiwan)	**None**	0%
Deposition (non-ICs)		$0.94 billion	Applied Materials (U.S.), Lam Research (U.S.), Evatec (Switzerland), ASM Pacific (China), AMEC (China), others	**High**	13.2%

Chemical vapor deposition. The United States,[132] the Netherlands, Japan, and South Korea are the primary producers of CVD tools, while China is gaining capabilities. CVD includes four types: plasma CVD, low pressure CVD (LPCVD), high temperature CVD (HTCVD),[133] and atomic layer deposition (ALD). CVD tools create a chemical vapor that deposits films on the wafer atom-by-atom or molecule-by-molecule. CVD is the most widely used deposition technique in chip fabrication. It is used to deposit most dielectrics (a type of insulator), silicon, and some metals. Capable of depositing layers a single atom in thickness, ALD is essential for leading-edge nodes.[134] China's Piotech produces plasma CVD tools for depositing dielectrics purportedly for the 5 nm node,[135] while SKY Technology Development produces it for low-volume R&D applications.[136] China's NAURA produces LPCVD tools for a wide number of applications.[137] Piotech

and NAURA both sell ALD tools for several applications at the 14 nm node and possibly more advanced.[138] China's capabilities are modest and insufficient to fully localize deposition, but are growing. Some areas of CVD are chokepoints for China, but it is unclear for how long.

Physical vapor deposition. The United States controls the PVD equipment market, with Japan capturing most of the rest. China and Switzerland both have small shares. PVD vaporizes a solid or liquid material, which then condenses onto a substrate. There are two main forms: "evaporation," rarely used in semiconductor manufacturing, and "sputtering," now the primary PVD method. Sputtering is a dominant method used for depositing conductors (like metals), but also sometimes used for dielectrics. China's NAURA has developed sputtering tools for key materials for ≥28 nm nodes.[139] SKY Technology Development also produces PVD tools.[140]

Rapid thermal processing. The United States, Japan, and South Korea solely produce RTP tools, which are a chokepoint for China. RTP tools include lamps, lasers, or other mechanisms to quickly increase the temperature of a wafer to change its properties. RTP is critical to several steps in chip manufacturing.[141] RTP tools include two submarkets: conventional tools provide heat for as long as multiple seconds (solely produced by the United States and South Korea); and other tools provide it only for milliseconds (solely produced by the United States and Japan).

Tube-based diffusion and deposition. Japan, the Netherlands, South Korea, China, and the United States produce tube diffusion tools, while only Japan and the Netherlands produce tube deposition tools. These systems are "tube"-based because substrates are loaded in cylindrical chambers for processing—which cause diffusion of dopants into a wafer in tube *diffusion* systems, and deposit materials for certain applications in tube *deposition* systems.[142] China's NAURA produces several tube diffusion furnaces for ≥28 nm nodes,[143] but China does not produce tube deposition tools.

Spin-coating. Japan is the major producer of spin-coating systems used in chip production. These tools spin a wafer to spread liquid material deposited on the wafer across it. Spin-coating is used extensively in photoresist coating but only for narrow applications in chip production.[144] China's Kingsemi sells lower-end spin-coating tools for photoresist deposition (see "photoresist processing" within "lithography" section) and a few other applications in chip manufacturing.[145] Given the niche use of spin- coaters in chip manufacturing and because China has at least some expertise, spin-coaters are not a major,

long-term chokepoint for China in chip manufacturing outside of photoresist deposition.

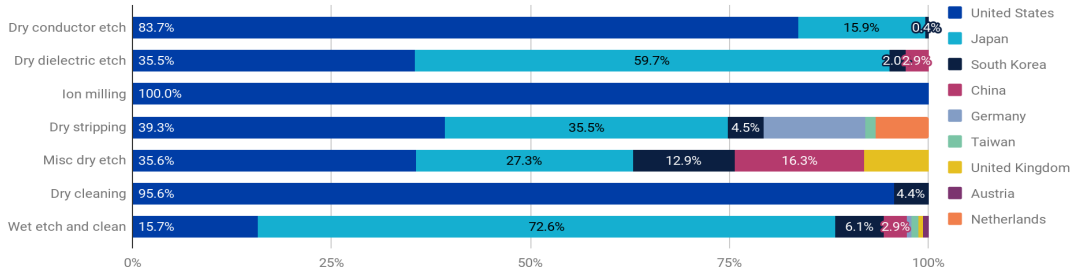
Electrochemical coating. Only the United States and Taiwan produce electrochemical coating tools.[146] A common application is to deposit copper (used for wiring in chips) across a wafer. However, other techniques, like CVD, can also deposit copper for some applications. Electrochemical coating tools would be important for China only if it cannot find a substitute tool to perform the same task.

Deposition (non-ICs). The United States and Japan are the biggest producers of deposition tools for the production of microelectromechanical systems (MEMS), disk drives, compound semiconductors, advanced packaging, and other items besides chips. China has a strong market share (13.2 percent) in this segment compared to its market share (1.8 percent) in the overall deposition market. AMEC and ASM Pacific are key Chinese producers in this area.[147]

Etch and Clean

The United States and Japan are the main producers of etch and clean equipment, while South Korea and China are other significant producers (Figure 19 and Table 12). Compared to the other major categories of equipment, China has made more progress in its development of etching tools. Therefore, only the most advanced etching tools—atomic layer etching tools—are a chokepoint for China.

Figure 19: 2019 etch, dry processing, and wet processing country shares by firm headquarters



Source: VLSI Research

Table 12: 2019 etch and clean market and Chinese competitiveness

Equipment		2019 market size	Top firms + Chinese firms	Chinese firm capabilities	Chinese market share
Dry etching	Conductor etching	$6.5 billion	Lam Research (U.S.), Applied Materials (U.S.), Hitachi (Japan), Tokyo Electron (Japan), NAURA (China), others	**High**: ≥5 nm for dielectrics; also has capabilities for conductors and other materials; except **none** for atomic layer etching	<1%
	Dielectric etching	$4.3 billion	Tokyo Electron (Japan), Lam Research (U.S.), AMEC (China), others		2.9%
	Misc. etching	$0.16 million	Plasma-Therm (U.S.), SAMCO (Japan), GigaLane (South Korea), NAURA (China), AMEC (China), others		16.3%
	Ion milling	$12 million	Veeco (U.S.)	**None**	0%
	Dry stripping	$0.33 million	Lam Research (U.S.), Hitachi (Japan), Mattson Tech (U.S.), PVA TePla (Germany), others		
Dry cleaning		$0.15 million	Lam Research (U.S.), Charm Engineering (South Korea)		
Wet etching and wet cleaning		$3.2 billion	Screen (Japan), Tokyo Electron (Japan), Lam Research (U.S.), Semes (South Korea), NAURA (China), Kingsemi (China), others	**Moderate**	<2%

Etching tools are responsible for creating permanent patterns in chips: after photolithography removes portions of a photoresist deposited on a wafer in a precise pattern, etching tools etch that pattern into a permanent substrate below. Cleaning tools then remove etched materials. Etching and cleaning tools have two main types: dry and wet. Dry etching tools—using gases to etch the substrate—are the most commonly used tool, and are especially necessary for circuit features at advanced nodes. Wet etching tools, using liquids, are less commonly used, and largely for cleaning wafers.[148]

Dry etch and clean. The United States and Japan are the main producers of dry etching and cleaning tools,[149] which South Korea, China, and other

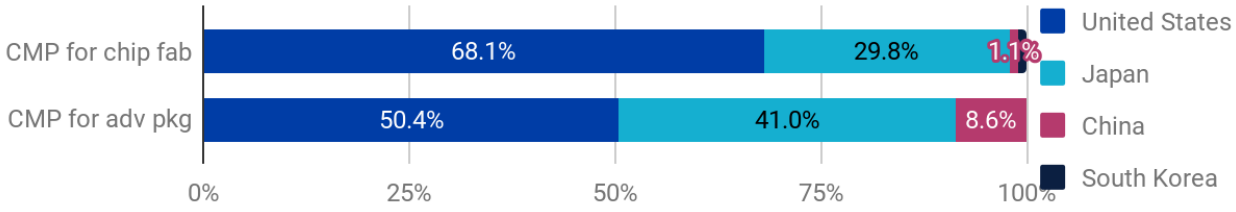
countries also produce. The main types of dry etching tools are used either for etching conductors or dielectrics.[150] Dry etching tools have advantages over wet tools: they are fast and can etch differently depending on the direction of etch,[151] which enables fine-grained features with complex shapes. Other types of dry etching tools are for specific, less critical uses: ion milling tools etch certain features on wafers, while dry stripping tools remove photoresists (though these functions can be performed with other tools). The most advanced dry etching tools are called atomic layer etching (ALE) tools. These tools are important for both conductor and dielectric etch of the smallest features in <10 nm nodes,[152] and are produced by leading U.S., Japanese, and British firms.[153] While ALE's market is currently only in the range of hundreds of millions of dollars, it could potentially be used to manufacture next-generation transistor structures.[154] China's AMEC produces dry etching tools that are perhaps the most advanced SME tools sold by any Chinese firm. They are used for leading Taiwanese chipmaker TSMC's 7 and 5 nm nodes,[155] though not for the finest features, such as in complex transistor structures. Other Chinese SME are typically used only by domestic fabs such as SMIC.[156] China's NAURA also produces dry etch tools for dielectrics, conductors, and silicon.[157] Recognizing China's competitiveness in dry etching tools, the United States removed them from the Commerce Control List in 2016.[158] China does not make ion milling, dry stripping, and dry cleaning tools, but these are lower-value and less advanced. China's key chokepoint is ALE tools, which it has yet to develop.[159] However, given its expertise in dry etching tools, AMEC is likely attempting to develop ALE tools.

Wet etch and clean. Japan and the United States are the main producers of wet etching and cleaning tools, with several other countries, including China, capturing some market share. Wet etching has advantages compared to dry etching—it is cheaper, risks less damage to substrates, and is more selective, i.e., it can etch a particular material without unintentionally etching nearby materials. However, it is slower and typically cannot etch differently depending on the direction of etch, making it difficult to form complex structures. Therefore, wet etching is not typically used for etching the smallest features in advanced chips. China's Kingsemi produces wet etching and cleaning tools,[160] while China's NAURA sells wet cleaning tools for ≥28 nm nodes.[161]

Chemical Mechanical Planarization

The United States and Japan are dominant producers of chemical mechanical planarization tools, while China and South Korea capture the remaining market share (Figure 20 and Table 13). After other steps like etching and cleaning, CMP tools flatten the wafer surface.[162] Hwatsing is China's top producer, both for fabrication and packaging applications. CMP tools are critical for chip fabrication, but not as complex as other tools, such as lithography and deposition tools. Hwatsing's CMP tools can process 300 mm wafers and are purportedly suitable for ≥14 nm nodes.[163] Therefore, CMP tools are not a critical chokepoint for China, except at the leading edge.

Figure 20: 2019 CMP country shares by firm headquarters



Source: VLSI Research

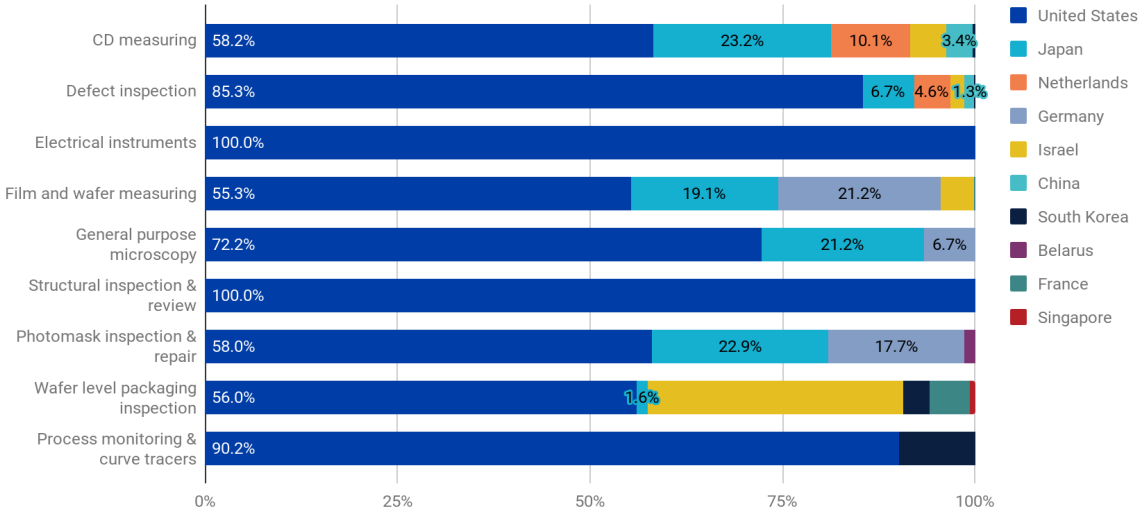
Table 13: 2019 CMP market and Chinese competitiveness

Equipment	2019 market size	Top firms + Chinese firms	Chinese firm capabilities	Chinese market share
CMP front end fab	$1.4 billion	Applied Materials (U.S.), EBARA (Japan) Accretech (Japan), Hwatsing (China), KCTech (South Korea), Revasum (U.S.), CETC (China)	**Moderate**: 300 mm wafers, ≥14 nm nodes	1.1%
CMP adv. packaging	$49 million			8.6%

Process Control

The United States[164] and Japan are the main producers of process control tools, with various other countries, including China, capturing small market shares (Figure 21 and Table 14). This market segment includes chokepoints for China, particularly within metrology and inspection equipment. Process control tools monitor wafers, photomasks, and the overall chip manufacturing process to ensure consistency and low manufacturing error rates.[165] Accordingly, they are among the most essential and valuable tools after lithography tools.[166]

Figure 21: 2019 process control country shares by firm headquarters



Source: VLSI Research

Table 14: 2019 process control market and Chinese competitiveness

Equipment		2019 market size	Top firms + Chinese firms	Chinese firm capabilities	Chinese market share
Wafer inspection	Film and wafer measuring	$0.54 billion	KLA (U.S.), Bruker (Germany), Rigaku (Japan), Screen (Japan), others	**Minimal**: optical film & CD measuring tools for 300 mm wafers, ≥14 nm	<1%
	Electrical instruments	$7 million	Onto Innovation (U.S.)		0%
	CD measuring	$1.6 billion	KLA (U.S.), Hitachi (Japan), ASML (Netherlands), Onto Innovation (U.S.), Applied Materials (U.S.), RSIC (China), others		3.4%
	Defect inspection	$3 billion	KLA (U.S.), Applied Materials (U.S.), Hitachi (Japan), ASML (Netherlands), RSIC (China), SMEE (China), others		1.3%
	General purpose	$0.2 billion	Thermo Fisher (U.S.), Hitachi (Japan), Zeiss (Germany),		0%

	microscopy		PVA TePla (Germany), Nanotronics (U.S.)		
	Structural inspection & review	$17 million	Thermo Fisher (U.S.)		0%
Photomask inspection & repair		$0.94 billion	KLA (U.S.), Lasertec (Japan), Zeiss (Germany), Applied Materials (U.S.), others	None	0%
Wafer level packaging inspection		$0.2 billion	CAMTEK (Israel), Onto Innovation (U.S.), others		0%
Process monitoring & curve tracers		$79 million	Keysight Tech (U.S.), Keithley Instruments (U.S.), Top Engineering (South Korea)		0%

Wafer inspection. The United States and Japan have dominant shares in wafer inspection tools, while China produces only some of the wafer inspection tools required for chip fabrication. The key sectors include electrical instruments[167] and tools for film and wafer measuring,[168] critical dimensions measuring,[169] defect inspection,[170] general purpose microscopy,[171] and structural inspection.[172] China's RSIC produces optical film measurement tools for measuring 300 mm wafers during deposition, lithography, etch, and CMP,[173] and optical critical dimensions measuring tools for advanced, complex features in 300 mm wafers.[174] RSIC also achieves some capabilities as advanced as 14 nm.[175] China's Grand Tec and SMEE also sell wafer inspection tools.[176] Overall, wafer inspection tools represent a chokepoint for China.

Photomask inspection and repair. Japan, Germany, and the United States produce almost all photomask inspection and repair tools. These tools are similar to those used in wafer inspection, such as microscopes. China does not produce these tools, therefore representing a chokepoint.

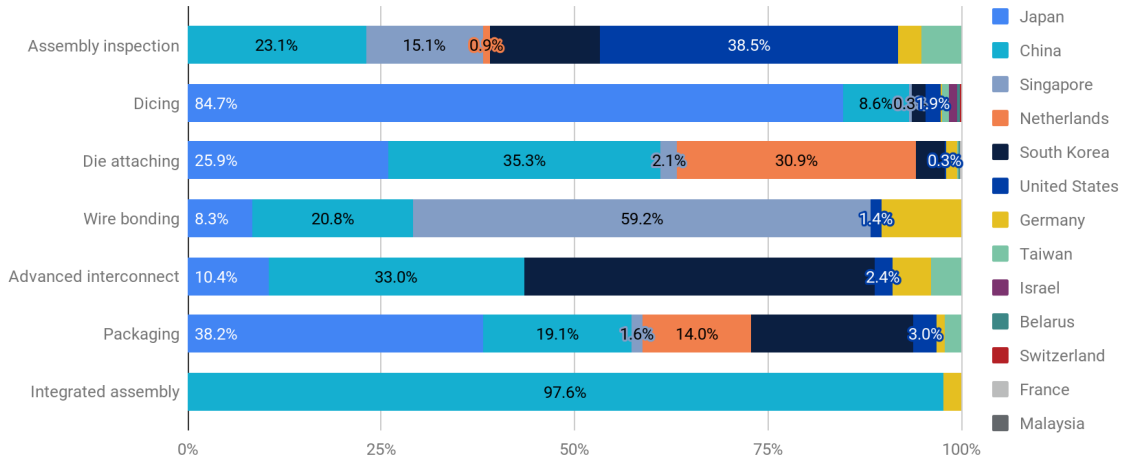
Wafer level packaging inspection. The United States and Israel primarily sell these tools, which inspect parts of wafers that package fabricated chips (dies) before these wafers are "diced" (i.e., cut) into multiple chips. As with other inspection tools, wafer level packaging inspection tools are a chokepoint for China.

Process monitoring and curve tracers. Only the United States and South Korea produce these tools. They measure performance of devices fabricated in wafers during the manufacturing to ensure normal operation. Relatively low value, they are unlikely to represent significant chokepoint for China.

Assembly and Packaging

Japan, China, Singapore, the United States, and a number of other countries produce assembly and packaging tools (Figure 22 and Table 15), taking a wafer with completed, unseparated chips and turning it into separate, packaged chips. These tools include assembly inspection tools,[177] dicing tools,[178] bonding tools,[179] packaging tools,[180] and integrated assembly tools.[181] Assembly and packaging tools represent the SME segment in which China is most competitive, with large market shares in most of these segments, particularly due to Hong Kong-based ASM Pacific.

Figure 22: 2019 assembly country shares by firm headquarters



Source: VLSI Research

Table 15: 2019 assembly market and Chinese competitiveness

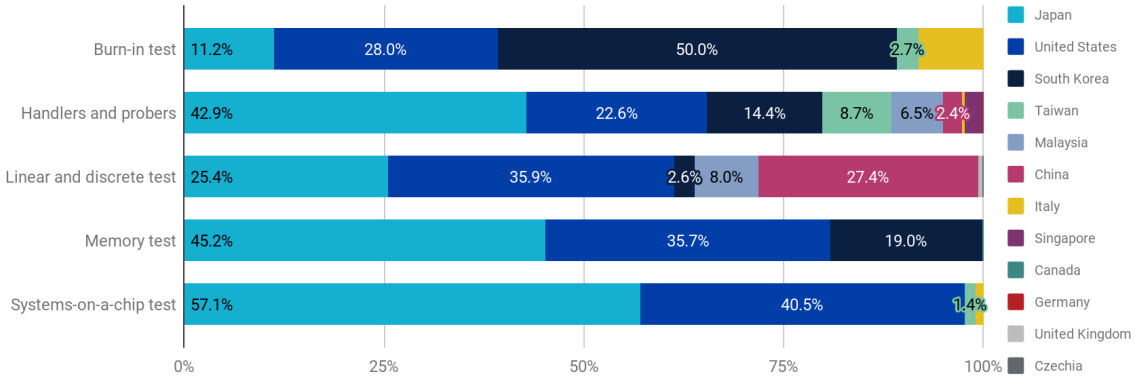
Equipment		2019 market size	Top firms + Chinese firms	Chinese firm capabilities	Chinese market share
Assembly inspection		$0.27 billion	KLA (U.S.), ASM Pacific (China), ASTI (Singapore), Koh Young Tech (South Korea), Cohu (U.S.), MIRTEC (South Korea), Grand Tec (China), others	**High**	23.1%
Dicing		$0.69 billion	DISCO (Japan), Accretech (Japan), ASM Pacific (China), Longhill (China), SYNOVA (China), others		8.6%
Bonding	Die attaching	$0.8 billion	Besi (Netherlands), ASM Pacific (China), Fasford Tech (Japan), Canon (Japan), Hoson (China), PROTEC (South Korea), JIAFENG (China), DIAS Automation (China), others		35.3%

	Wire bonding	$0.55 billion	Kulicke & Soffa (Singapore), ASM Pacific (China), Hesse (Germany), Shinkawa (Japan), JIAFENG (China), DIAS Automation (China), others		20.8%
	Advanced interconnect	$68 million	ASM Pacific (China), SSP (South Korea), KOSES (South Korea), DIAS Automation (China), others		33.0%
Packaging		$0.55 billion	TOWA (Japan), ASM Pacific (China), Besi (Netherlands), HANMI (South Korea), Trinity Tech (China), Grand Tec (China), DIAS Automation (China)		19.1%
Integrated assembly		$34 million	ASM Pacific (China), Grohmann (Germany)		97.6%

Testing

Japan, the United States, and South Korea produce most testing tools, while China has only a small market share (Figure 23 and Table 16). These include testing tools for memory chips, systems-on-a-chip,[182] linear and discrete devices,[183] burn-in tools,[184] and handlers and probers.[185] China's firms are largely limited to lower-end segments, especially for testing lower-end linear and discrete devices. They do not have a significant presence in advanced logic and memory chip testing tools—a notable chokepoint. However, some U.S. firms have major presences in China,[186] and Chinese firms are also acquiring foreign testing tool firms.[187] Therefore, China has opportunities to become more competitive.

Figure 23: 2019 testing country shares by firm headquarters



Source: VLSI Research

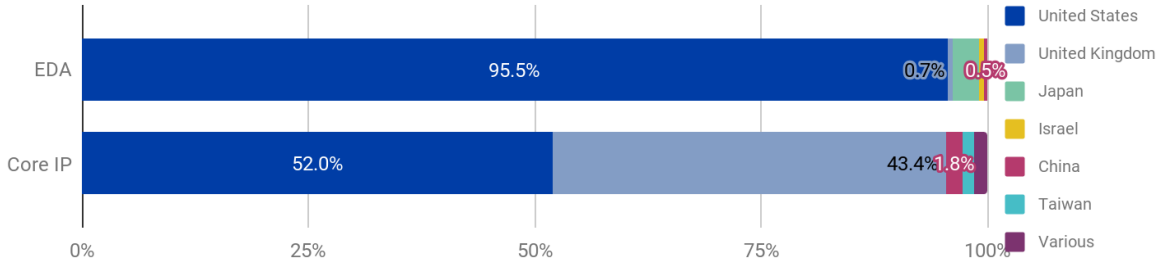
Table 16: 2019 testing market and Chinese competitiveness

Equipment	2019 market size	Top firms + Chinese firms	Chinese firm capabilities	Chinese market share
Memory test	$0.67 billion	Advantest (Japan), Teradyne (U.S.), UniTest (South Korea), others	**None**	0%
SoC test	$2.7 billion	Advantest (Japan), Teradyne (U.S.), COHU (U.S.), others		
Burn-in test	$0.22 billion	UniTest (South Korea), DI (South Korea), Micro Control (U.S.), others		
Linear and discrete test	$96 million	National Instruments (U.S.), TESEC (Japan), AccoTEST (China), Hoson (China), Shanghai Juno (China), others	**High**	27.4%
Handlers & probers	$1.8 billion	Accretech (Japan), Cohu (U.S.), Tokyo Electron (Japan), ASM Pacific (China), Grand Tec (China), JHT (China), others	**Moderate**	2.4%

Electronic Design Automation and Core IP

The United States is the dominant producer of electronic design automation software, and the United States and the United Kingdom are dominant producers of core intellectual property. These interrelated inputs into chip design are both key chokepoints for China (Figure 24 and Table 17).

Figure 24: EDA and core IP country shares by firm headquarters



Source: Mentor Graphics, Journal of Microelectronic Manufacturing, IPNest, BCG[188]

Table 17: 2019 EDA and core IP market and Chinese competitiveness

Segment	2019 market size[189]	Top firms + Chinese firms	Chinese firm capabilities	Chinese market share
EDA software	$6.8 billion	Synopsis (U.S.), Cadence (U.S.), Mentor Graphics (U.S./Germany),[190] Ansys (U.S.), Silvaco (U.S.), PDF Solutions (U.S.), Huada Empyrean (China), Primarius (China), Xpeedic (China), Semitronix (China), Platform-da (China), Microscapes (China), Arcas-da (China), others	**Low**	0.5%
Core IP	$3.9 billion	ARM (U.K./Japan),[191] Synopsys (U.S.), Cadence (U.S.), SST (U.S.), Imagination Technologies (U.K./China), Ceva (U.S.), Verisilicon (China), Achronix (U.S.), Rambus (U.S.), eMemory Technology (Taiwan), others	**Low**	1.8%

EDA software. U.S. firms are the exclusive providers of EDA software with the full-spectrum capabilities needed by engineers at fabless firms and IDMs to design leading-edge chips.[192] U.S. firms also dominate capabilities relevant to AI chip design, such as ASIC layouts.[193] Although the industry is top-heavy, startups frequently enter the EDA space. However, they struggle to compete with top EDA firms that typically acquire them to incorporate the startups' niche functionality to their full-spectrum capabilities.[194]

China's EDA industry is small. Only 300 engineers work in it, as compared to 1,500 total EDA engineers in China (counting foreign multinationals' employees), and Synopsys' EDA engineering workforce of more than 5,000.[195] Empyrean, founded in 2009, is China's leading EDA firm.[196] Empyrean is purportedly the only Chinese EDA firm that can run a complete design flow. Its tools can fully design certain analog and mixed-signal (a combination of analog and digital) chips.[197] The company has a particular niche in the design of chips for flat-panel displays. Customers include China's top chip design firms, including HiSilicon, and various foreign customers. Samsung uses Empyrean's EDA tools for flat-panel displays.[198]

Outside of Empyrean's niche offerings, Chinese chip designers rely on U.S. EDA tools—especially Synopsys and Cadence—for all chip designs. The remainder of China's EDA tools support only narrow slices of the chip design flow or supplement leading U.S. EDA tools.[199] Even these capabilities largely do not support leading-edge fabrication processes (e.g., ≤14 nm).[200] Leading chipmakers Intel, Samsung, and TSMC give the top U.S. EDA firms, such as Synopsys and Cadence, preferential access to process IP during the development of new manufacturing processes. Each chipmaker's manufacturing process uniquely limits chip design options available to chip designers. Chinese EDA firms may later access process IP that is either incomplete or without sufficient support. As long as this tiered-access continues, Chinese EDA firms will be unable to support chip designs at leading-edge nodes nor compete with the top U.S. EDA firms.[201] However, this situation is changing. Several Chinese EDA startups have attracted executives and technologists from U.S. leaders.[202] Additionally, DARPA programs are developing open-source EDA tools that can run full design flows for some applications, which chip designers worldwide can use.[203]

Core IP. Chip design firms license core IP, which consists of reusable design blocks, and incorporate it final chip designs. U.S. and U.K. vendors dominate the market. Some firms specialize exclusively on core IP, such as U.K.-based,

Japanese-owned ARM, while others combine their offerings with EDA tools. ARM is the top core IP vendor, providing an instruction set architecture (ISA) and associated core IP underpinning most of the world's smartphone processors. U.S.-based Nvidia offered to acquire ARM. If the deal passes regulatory scrutiny, it would expand U.S. jurisdiction over ARM—and give U.S.-headquartered firms over 90 percent market share in core IP.

China is weak in core IP development, but acquisitions, joint ventures, and open-source development give China opportunities to increase capabilities. In 2017, a Chinese state-owned fund acquired U.K.-based Imagination Technologies, which develops core IP for many types of chips, for mobile GPUs.[204] And ARM China, 51 percent owned by Chinese investors and 49 percent by U.K.-based ARM Holdings, accounts for 27 percent of ARM's global licensing revenues.[205] Chinese chip designers could build on the open-source architectures RISC-V and MIPS—success could take years, but it would eliminate China's reliance on proprietary U.K. and U.S. core IP.[206]

For now, Chinese chip designers are heavily reliant on non-Chinese core IP. Ninety-five percent of Chinese chips incorporated IP licensed from ARM.[207] For example, leading chips used in smartphones are largely based on ARM's instruction set architecture (ISA) and core IP. Huawei's subsidiary HiSilicon—China's top fabless design firm—also relies on ARM's ISA and core IP.[208]

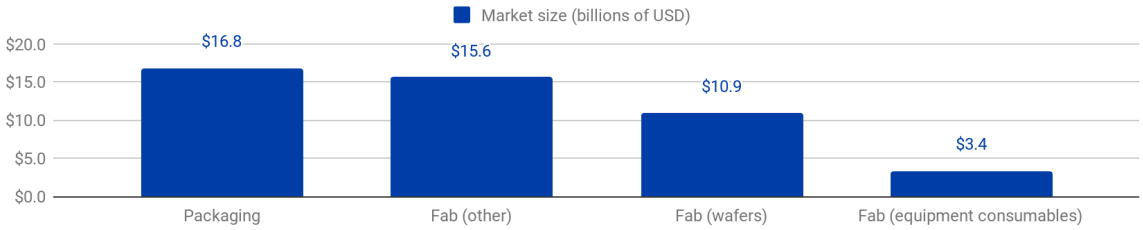
Materials

Chinese firms are dominant suppliers of raw materials, but face multiple chokepoints in the production of manufactured materials (which take many materials as inputs) used in semiconductor manufacturing. Chokepoints include advanced 300 mm wafers, photomasks, and photoresists. Meanwhile, the United States has a small domestic production capacity and relies heavily on imports for raw materials, but does have meaningful market share across semiconductor material segments.[209] Together, the United States and its allies control a large share of global production capacity for the vast majority of raw materials[210] and an exclusive share for certain semiconductor materials.

The following subsections first cover raw materials, then the materials segments highlighted in Figure 25, which shows the 2019 semiconductor materials market categorized by stages in semiconductor production. Each semiconductor materials segment takes raw materials as inputs. The production stages include materials used in the production of wafers

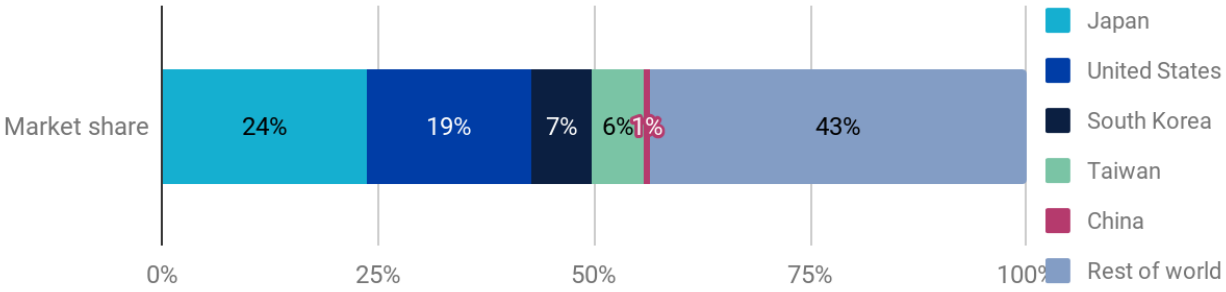
(predominantly silicon wafers), fab materials used to manufacture chips (including materials used to form chip features and consumables used by SME), and packaging materials. The market for materials used in semiconductor production was $46.8 billion in 2019.[211] Figure 26 provides country market shares for semiconductor materials.

Figure 25: 2019 semiconductor materials market



Source: Techcet[212]

Figure 26: Semiconductor materials country shares by firm headquarters



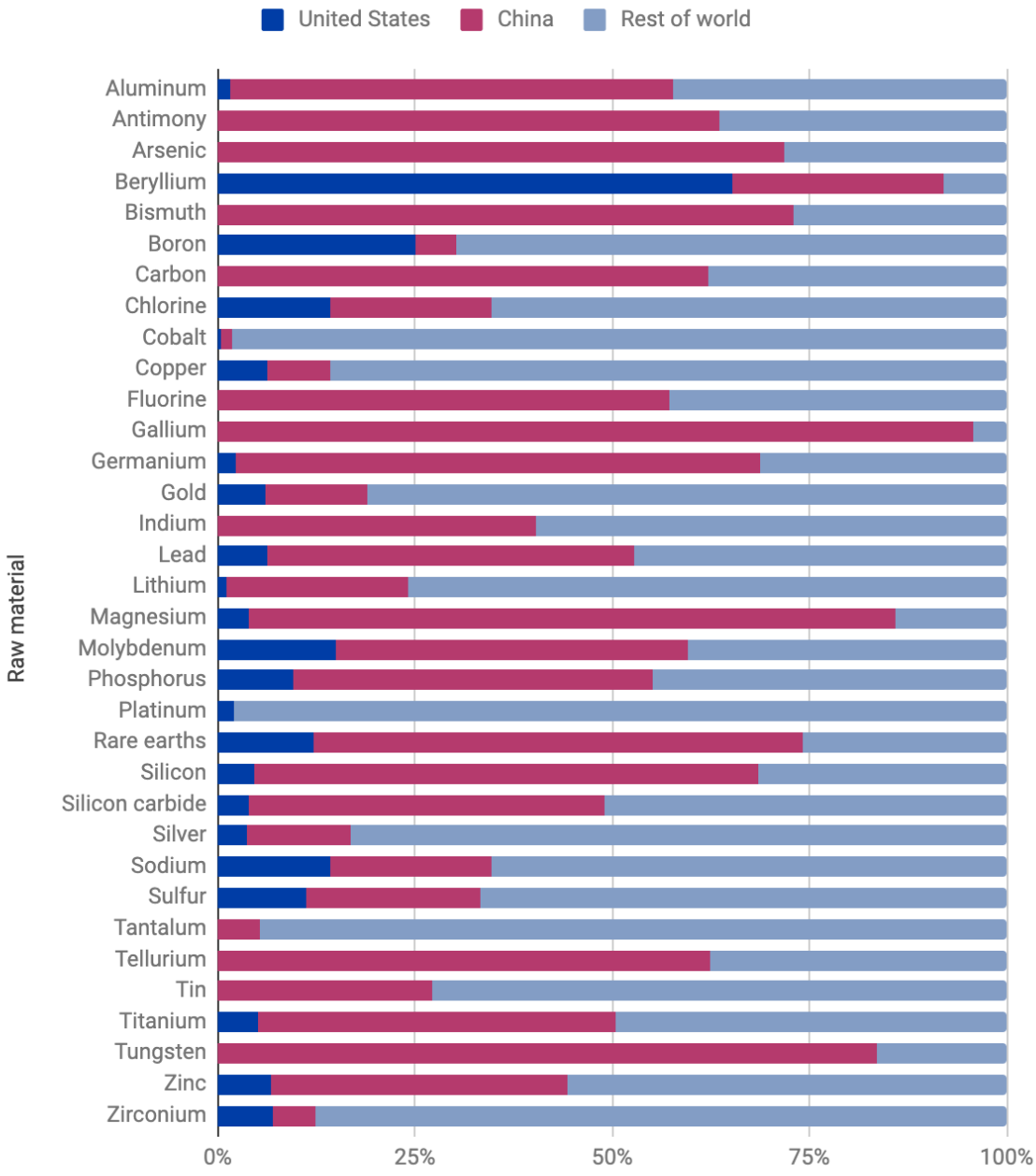
Source: Bain, WIPO[213]

Raw Materials

China is the world's breadbasket for raw materials, while the United States and its allies together also produce a sizable share of nearly all materials. Given the complexity of semiconductor fabrication, the raw materials that go into these segments span a large portion of the periodic table. Figure 27 shows U.S., Chinese, and the rest of the world's primary production share for raw materials. This figure largely covers the most key non-gaseous materials, but not exhaustively.[214] "Primary" production refers to mining of materials, especially low-grade materials before processing into high-grade materials or into compound forms.

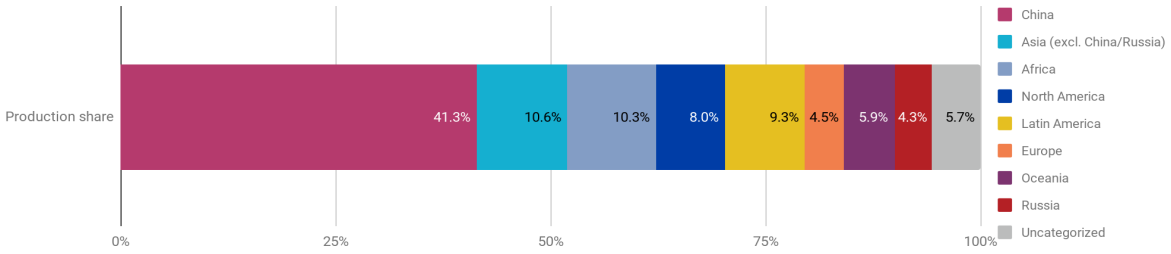
China has the largest share for most materials, and a significant share for all but cobalt (1.4 percent) and platinum (0 percent). The United States produces a small amount of most materials, but produces no antimony, arsenic, carbon, fluorine, gallium, indium, tantalum, tellurium, tin, or tungsten. But together, the United States and its allies produce a sizable share of all materials—except for China's 95.7 percent production share for primary low-grade gallium, 83.6 percent production share for tungsten, and 82.0 percent production share for magnesium. China has a 64.0 percent production share for silicon—the most widely used material—but the United States and its allies have large reserves.[215] Although China no longer holds monopoly on rare earth mining, it still dominates rare earth processing.[216] Figure 28 takes an unweighted average of production shares of all of these materials and presents regional production shares.

Figure 27: 2019 primary production of raw materials by country/region



Source: USGS[217]

Figure 28: 2019 total material production share by country/region (unweighted average)



Source: USGS, CSET calculations[218]

Fab Materials

Japan, the United States, Taiwan, South Korea, and Germany are key producers of fab materials. China cannot produce leading-edge photomasks and photoresists and has limited capacity in producing 300 mm wafers. It also has middling capabilities in the production of other fab materials: chemical mechanical planarization (CMP) materials, deposition materials, electronic gases, and wet chemicals.[219] Table 18 summarizes these materials segments.

Table 18: Fab materials market

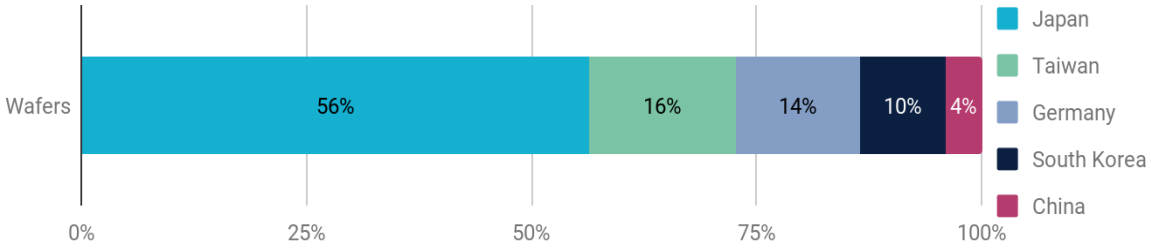
Materials	Market size	Key firms	Chinese firm capabilities	Chinese market share
Wafers	$10.9 billion	Shin-Etsu (Japan), SUMCO (Japan), GlobalWafers (Taiwan), Siltronic (Germany), SK Siltron (South Korea),[220] Okmetic (China),[221] JRH (China), Zhonghuan (China), Gritek (China), MCL (China), Simgui (China), GuoSheng (China), POSHING (China), and ZingSEMI (China)	**Low**: moderate for 200 mm wafers, but low for 300 mm wafers	<5% (<1% for 300 mm wafers)
Photomasks	$4 billion[222]	Dai Nippon (Japan), Photronics (U.S.), Toppan Photomasks (Japan), Hoya Corporation (Japan), Taiwan Mask Corporation (Taiwan), Intel (U.S.), Samsung (South Korea), TSMC (Taiwan), GlobalFoundries	**Moderate**: 28 nm photomasks	<5%

		(U.S.), SMIC (China), Shenzen Newway (China)		
Photoresists	$3.3 billion.[223]	JSR (Japan), Tokyo Ohka Kogyo (Japan), Shin-Etsu Chemical (Japan), Fujifilm Electronic Materials (Japan), Sumitomo Chemical (Japan), Dongjin (South Korea), DuPont Electronic Solutions (U.S.), EMD Performance Materials (U.S.), Inpria (U.S.), Ruihong (China), Kempur (China), Nata Opto-electronic Material (China), JHM (China)	**Low:** 150 nm KrF resists; developing ArF and ArFi resists; no EUV resists	<5%
Chemical mechanical planarization (slurries and pads) [224]	$2.5 billion	FujiFilm (Japan), Fujimi (Japan), Hitachi Chemical (Japan), Eminess Saint-Gobain (France), Versum Materials (U.S.), DuPont (U.S.), Cabot Microelectronics (U.S.), Thomas West (U.S.), JSR (Japan), Merck (Germany), CMC (U.S.), Anji (China), Hubei Dinglong (China)	**Low**	<5%
Deposition (sputtering targets)	$1 billion[225]	JX Nippon (Japan), Honeywell Electronic Materials (U.S.), Tosoh SMD (Japan), Linde (Germany), Praxair (U.S.), KFMI (China), Grikin (China)	**Moderate**	11%
Electronic gases[226]	$6 billion[227]	Merck (Germany), Entegris (U.S.), Air Products (U.S.), Air Liquide (France), Praxair (U.S.), Linde (Germany), BASF (Germany), TNSC (Japan), Showa Denka (Japan), Wonik (South Korea), SK Materials (South Korea), Nata Opto-electronic Material (China), Haute Gas (China), Jinhong Gas (China), PERIC (China)		Not available
Wet chemicals	Unavailable	KMG Chemicals (U.S.), BASF (Germany), Avantor (U.S.), Honeywell (U.S.), Kanto Chemical (Japan), Runma (China), JHM		

		(China), Jiangyin Chemical Reagents (China), Sinophorus (China), Sinyang (China), Etching Liquid (China)		

Wafers. Firms headquartered in Japan, Taiwan, Germany, and South Korea are top producers of wafers (Figure 29), especially 300 mm wafers, which China only minimally produces. China mostly imports wafer manufacturing equipment, so 300 mm wafers and this equipment together represent a significant chokepoint for China. There are no major U.S.-headquartered wafer producers, but some non-U.S. firms produce wafers in the United States.[228] Wafers are thin, disc-shaped materials on which chips are fabricated. Using specialized wafer manufacturing equipment, wafers can be made of different semiconductive materials.[229] These materials include silicon[230] or various other materials.[231] Most wafers are made purely of silicon or another material, but others have more complex structures.[232] Dopants are materials added to wafer materials (like silicon) to give them a level of semiconductivity suitable for transistors in chips to operate correctly.[233]

Figure 29: Wafer country shares by firm headquarters

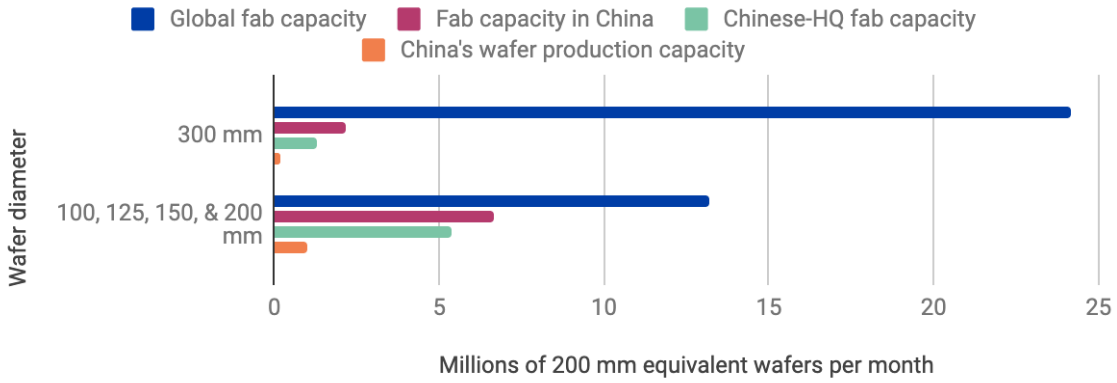


Source: CSET estimates based on financial statements and wafer production capacities

Wafer producers headquartered in Japan, Taiwan, Germany, and South Korea make state-of-the-art 300 mm diameter wafers, which are used for 99.7 percent of the world's fab capacity capable of manufacturing chips at ≤45 nm nodes.[234] Manufacturing the smoothest, high-purity 300 mm wafers—which are necessary for supporting the smallest chip features sizes—requires considerable tacit know-how.[235] Older-technology wafer sizes include 150 and 200 mm, used for chips with older, larger nodes. Chinese wafer producers generate little revenue in comparison. Of these, as of 2018, JRH, Zhonghuan, Gritek, Simgui, and ZingSEMI were producing or had plans to produce 300 mm wafers.[236] Figure 30 shows, for 100–200 mm fabs and 300 mm fabs, wafer fab capacity of the world, fabs in China, Chinese-

headquartered fabs (which are all in China), and China's current or planned wafer production capacity as of 2018. Chinese wafer producers respectively produce 18 percent and 12 percent of the wafers for Chinese-headquartered 100–200 mm fabs and 300 mm fabs. Therefore, China is especially reliant on imports for 300 mm wafers, and likely even more so for the most advanced 300 mm wafers.

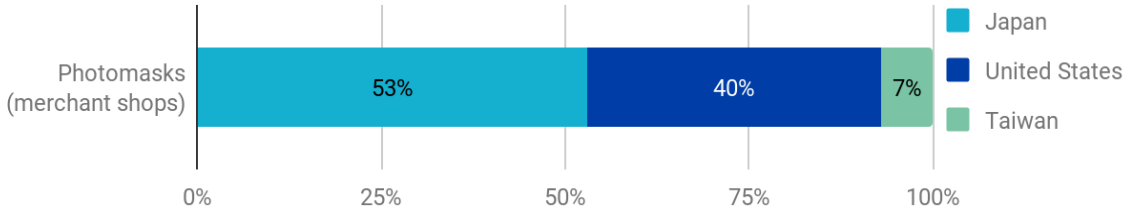
Figure 30: China's wafer production supply vs. demand



Source: SEMI, CSET calculations[237]

Photomasks.[238] Japan, the United States, Taiwan, and South Korea lead production of leading-edge photomasks (e.g., ≤16 nm), which China does not produce. China must import photomasks and mask-making equipment (electron-beam lithography and laser lithography tools), representing a major chokepoint. Photomasks are transparent plates containing a circuit pattern to be fabricated in a chip. Photolithography equipment produces light that passes through this pattern so that the photomask's pattern is transferred to the chip.[239] Each photomask is specific to one chip design (itself specific to a node). Photomasks are produced by captive mask shops (businesses within large semiconductor manufacturing firms) or merchant mask shops (which sell to semiconductor manufacturers).[240] In 2017, captive mask shops held 65 percent of market share.[241] Captive mask shop owners include leading chipmakers such as Intel (U.S.), Samsung (South Korea), TSMC (Taiwan), GlobalFoundries (U.S.), and China's leading chipmaker, SMIC,[242] which makes masks suitable for chips at ≥28 nm nodes.[243] But this transistor size is nearly a decade behind the state of the art. Japanese, U.S., and Taiwanese firms control the merchant mask shop market (Figure 31). China's merchant mask shop Shenzen Newway is not competitive with international leaders.

Figure 31: Merchant mask shop country shares by firm headquarters



Source: CSET estimates based on financial statements

Photoresists. Japan dominates the production of semiconductor photoresists with 90 percent market share,[244] with the remainder largely held by U.S. and South Korean firms.[245] China cannot produce the most advanced photoresists. Photoresists are chemicals deposited on a wafer that, when exposed to patterned light passing through a photomask, selectively dissolve to form the circuit pattern. Etching is then performed in places where the photoresist has dissolved to transfer the circuit pattern permanently onto the wafer.[246] Photoresists are specific to particular photolithography processes, such as EUV, ArF immersion, ArF, KrF, and i-line.[247] China's Ruihong sells i-line photoresists suitable for ≥350 nm nodes. Ruihong had $21 million in revenue in 2017, representing less than 1 percent of the photoresist market. Kempur is further along, having introduced KrF photoresists suitable for ≥150 nm nodes.[248] Chinese firms, particularly Nata, are also developing dry ArF and ArF immersion photoresists suitable for up top 28 nm nodes.[249] Ultimately, China remains reliant on imports,[250] as Chinese firms lack experience, know-how, and production technology, and have limited access to certain raw materials.

Chemical mechanical planarization materials. The United States, Japan, France, and China produce CMP materials. CMP is a process that makes layers produced during fabrication flat so lithography can successfully be performed on them. The highest-value materials used in CMP are chemical slurries and polishing pads.[251] During fabrication, a wafer is placed on the pad along with the slurry,[252] and a polishing head presses against the wafer and rotates to planarize the wafer. The CMP slurry market is sized at $790 million. Two U.S. firms, Dupont and Cabot Microelectronics, control about 56 percent of CMP slurry market share. Another 34 percent is controlled by other U.S., Japanese, and French firms.[253] A remaining 10 percent covers others, including the Chinese firm Anji, which had about $31 million in revenue in 2017, good for about 4 percent of the market.[254] Anji produces slurries suitable for depositing many key materials,[255] but cannot produce

high-end slurries. The CMP pad market is sized at $1.7 billion. As of 2014, DuPont (U.S.) had 78 percent market share, with Fujibo (Japan) and Cabot (U.S.) each having 4 to 6 percent. However, the Chinese firm Hubei Dinglong now also produces CMP pads.[256]

Deposition materials. The United States and Japan are key producers of deposition materials, but China has the ability to produce many of these materials as well. Chemical vapor deposition (CVD) is the most common deposition method. Physical vapor deposition (PVD) is another. One form called sputtering fires argon ions on a target, whose atoms are stripped off and deposited as a thin film on the wafer.[257] As of 2014, JX Nippon (Japan) had 55 percent share in the production of sputtering targets, with other major providers including Honeywell Electronic Materials (U.S.), Tosoh SMD (Japan), and Praxair (U.S.).[258] Chinese companies KFMI and Grikin have been gaining market share for years, especially at the expense of Tosoh and Praxair. KFMI had a 2017 revenue of $78 million and Grikin had a 2017 revenue of $34 million.[259] Many materials used in deposition are also simply purified versions of raw materials that China mines abundantly.

Electronic gases. The United States, France, Japan, Germany, and China all produce electronic gases, which are widely used in semiconductor fabrication.[260] Merck (Germany), Air Products (U.S.), and Air Liquide (France) lead the market.[261] China's Nata Opto-electronic Material had $5 million in semiconductor materials revenue in 2017, significantly derived from electronic gases, including precursors for chemical vapor deposition and atomic layer deposition. China's Haute Gas makes a variety of gases with $130 million in revenue in 2017, a subset of which is electronic gases. Jinhong Gas and PERIC are other Chinese electronic gas producers.[262]

Wet chemicals. The United States, Germany, and Japan are top producers of wet chemicals, used widely in semiconductor fabrication. More than 60 percent of market share is held by KMG Chemicals (U.S.), BASF (Germany), Avantor (U.S.), Honeywell (U.S.), and Kanto Chemical (Japan).[263] China has a number of producers.[264] Runma sells hydrogen fluoride, nitric acid, and other chemicals. JHM sells certain high purity chemicals, with a 2017 revenue of $50 million. Jiangyin Chemical Reagents also sells various high purity chemicals. Sinophorus sells phosphoric acid and etching liquids. Finally, Sinyang sells chemicals and Etching Liquid sells various chemical solutions with a 2017 revenue of $30 million.[265]

Packaging Materials

Japan leads production of packaging materials, while other countries including the United States and China also have market shares (Table 19). Packaging involves several steps to bond a fabricated chip to an encasing package. For example, a bond wire attaches the chip to a lead frame.[266] The lead frame transfers data between the chip and external devices.[267] A protective ceramic package, plastic substrate, or encapsulant resin can also be bonded to the chip.[268] Die attach materials including polymers and eutectic alloys are used to attach the chip to packages or substrates.[269]

Table 19: Packaging materials market[270]

Materials	Market size	Key firms	Chinese firm capabilities
Lead frames	$16.8 billion	SH Material (Japan), Mitsui High-Tec (Japan), ASM Pacific (China), Shinko (Japan), Kangqiang (China), Hualong (China), Trinity (China), Yongzhi (China)	Stamping, etching, and plating leadframes
Bond wires		Heraeus (Japan), Tanaka Denshi (Japan), Nippon Micro (Japan), Doublink (China), Kangqiang (China), YesDo (China), KDDX (China)	Gold, copper, palladium-copper, silver, aluminum
Ceramic packages		Amkor (U.S.), Quik-Pak (U.S.), NGK (Japan), Alent (U.K.), Hitachi (Japan), Kyocera (Japan), LG (South Korea), Sumitomo (Japan), BASF (Germany) , Mitsui High-Tec (Japan), Henkel (Germany), Toray (Japan), Tanaka (Japan), Zhongwei (China), Yixing (China)	Packages for chips, modules, MEMS
Substrates		Ibiden (Japan), NanYa (Taiwan), Shinko (Japan), Samsung (South Korea), Shennan Circuits (China), Zhuhai Yueya (China), AKM (China)	Ball grid arrays, chip-scale packages, package for flexible circuits
Encapsulation resins		Sumitomo (Japan), Henkel (Germany), Hitachi (Japan), Sinopaco (China), HHCK (China)	Mold compounds
Die attach materials		Henkel (Germany), Hitachi (Japan), Sumitomo (Japan), Darbond (China), Hysol Huawei (China), Y-Bond (China)	Die attach materials

Conclusion

Complex and globalized supply chains have driven rapid progress in semiconductors for decades—epitomized by Moore's Law. Today, semiconductors represent a critical strength for the United States, which remains the global leader across many parts of the supply chain. Together, the United States and its allies—especially Japan, the Netherlands, Taiwan, South Korea, the United Kingdom, and Germany—are technological and market leaders at virtually every step of the semiconductor supply chain.

Though still lagging behind, China increasingly challenges this leadership across several sectors. In particular, China is quickly expanding market share in chip design and manufacturing; and also plans to increase capabilities in production inputs: SME, EDA, core IP, and materials. If successful, China could reconfigure global supply chains, with critical impacts on U.S. national and international security. Companion CSET policy briefs titled "Securing Semiconductor Supply Chains"[271] and "China's Progress in Semiconductor Manufacturing Equipment"[272] offer recommendations to sustain U.S. and allied advantages—which will be at risk without concerted action.

Appendix A: Value Add of Supply Chain Segments

This appendix calculates the value add of each semiconductor supply chain segment using 2019 industry revenues.

Initially, we calculate the 2019 semiconductor market size of $444.5 billion by summing fabless chip sales ($106.6 billion), IDM chip sales ($251.8 billion), and OSD sales ($86.1 billion).[273] As shown in Table 20, we then allocate the semiconductor market to three production steps: design, fabrication, and ATP. We calculate the 2018 ATP market size of $53.4 billion by multiplying the 2019 OSAT market size ($28.2 billion)[274] by the 2017 ratio of total ATP market and OSAT market.[275] We calculate the 2019 fabrication market size of $248.1 billion by summing: (1) foundry services purchased by fabless firms ($59.5 billion), calculated by multiplying foundry revenue ($70.0 billion)[276] by the percentage of foundry services purchased by fabless firms (85%);[277] and (2) fabrication market size used by IDMs producing chips and OSD ($188.6 billion), calculated by multiplying foundry services purchased by fabless firms ($59.5 billion) by the ratio of combined IDM chip and OSD sales ($337.9 billion) and fabless chip sales ($106.6 billion). We calculate the 2019 design market size ($143.0 billion) by subtracting the calculated fabrication and ATP market sizes from the calculated semiconductor market size.

Table 20: 2019 value add of semiconductor production steps

Segment	Design	Fabrication	ATP	Total
Value add (USD billions)	$143.0	$248.1	$53.4	$444.5

Firms performing design, fabrication, and ATP source production inputs for each of these steps. As shown in Table 21, we divide each of these steps into multiple supply chain segments, each including a services portion and production inputs. Design firms purchase EDA and core IP, fabrication firms purchase equipment and materials, and ATP firms purchase equipment and packaging materials (market sizes from Table 17 and Figures 13 and 25).[278] The market sizes of these production inputs represent value added. After subtracting value add of these inputs from value add of production steps, we are left with value add for design services, fabrication services, and ATP services. Each value add is converted to a percentage by dividing by the 2019 semiconductor market size.

Table 21: 2019 value add of supply chain segments

Production step	Supply chain segments	Value add (USD billions)	Value add (%)
Design	Design services	$132.3	29.8%
	EDA	$6.8	1.5%
	Core IP	$3.9	0.9%
Fabrication	Fabrication services	$151.8	34.1%
	Fabrication equipment	$66.4	14.9%
	Fabrication materials (wafers)	$10.9	2.4%
	Fabrication materials (other)	$19.0	4.3%
ATP	ATP services	$26.0	5.8%
	ATP equipment	$10.6	2.4%
	Packaging materials	$16.8	3.8%

Appendix B: Glossary

Application-specific integrated circuits (ASICs) are logic chips with designs specialized for certain applications.

Assembly and packaging takes a wafer with completed, unseparated chips and turns it into separate, packaged chips.

Central processing units (CPUs) are the general purpose logic chips suited to perform a wide variety of calculations.

Chips, also called integrated circuits, each include a set of electrical circuits—made of small devices called transistors—in a flat piece made of a semiconductive material such as silicon. Logic chips perform calculations on digital data (zeroes and ones) to produce outputs. Memory chips store the digital data with which logic chips perform calculations.

Core intellectual property (IP) consists of reusable modular portions of chip designs that can be incorporated into complete chip designs.

Crystal growing furnaces and machining tools are used to produce wafers.

Chemical mechanical planarization (CMP) flattens wafer surfaces after other fabrication steps like etching and cleaning.

Cleaning removes materials from a wafer such as materials left over after being etched off of a wafer.

Deposition adds thin films of materials on a wafer to become parts of chips. Techniques include chemical vapor deposition, physical vapor deposition, electrochemical coating, spin-coating, rapid thermal processing, and tube-based diffusion and deposition.

Design determines the layout of transistors and wiring on a chip to be manufactured.

Discrete semiconductors each include only a single electrical device, such as a transistor, unlike a chip, which includes many interconnected devices forming circuits.

Dynamic random-access memory (DRAM) is a memory chip that stores data while a computer operates, but loses it when the computer powers down.

Electronic design automation (EDA) software is used to design chips.

Electronic gases are materials used in semiconductor fabrication.

Etching tools are responsible for creating permanent patterns in chips: after photolithography removes portions of a photoresist deposited on a wafer in a precise pattern, etching tools etch that pattern into a permanent substrate below. Dry and wet etching respectively use gas and liquid for etching.

Fabless firms design and sell chips, but buy chip manufacturing services from foundries and assembly, test, and packaging services from outsourced semiconductor assembly and test firms.

Fabrication turns designs into chips, relying on various semiconductor manufacturing equipment and fab materials.

Field-programmable gate arrays (FPGAs) are logic chips that can be reprogrammed after deployment to suit specific calculations.

Foundries are semiconductor manufacturing facilities that manufacture chips for third-party customers.

Graphics processing units (GPUs) are specialized logic chips used most commonly for graphics processing and developing artificial intelligence algorithms.

Lithography draws patterns in chemicals (such as photoresists) deposited on a wafer in a precise pattern. Techniques include photolithography, electron-beam lithography, laser lithography, and ion-beam lithography.

Integrated device manufacturers (IDMs) are firms that perform all three steps of production: design; fabrication; and assembly, testing, and packaging.

Ion implanters embed impurities (called dopants) into parts of wafers to change their properties.

NAND flash is a memory chip that stores memory permanently, even when power is turned off.

Outsourced semiconductor assembly and test (OSAT) firms perform assembly, testing, and packaging for third-party customers.

Packaging bonds a fabricated chip to an encasing package.

Photomasks are transparent plates containing a circuit pattern that photolithography tools pass light through to transfer the pattern to the chip.

Photoresists are chemicals deposited on a wafer that selectively dissolve to form the circuit pattern when exposed to patterned light that has passed through a photomask after generation by a photolithography tool.

Process control tools monitor wafers, photomasks, and the overall chip manufacturing process to ensure consistency and low manufacturing error rates. These include tools to inspect wafers, photomasks, and wafer level packaging; and process monitoring and curve tracers to measure performance of devices fabricated in wafers during the manufacturing to ensure normal operation.

Resist processing tools (also called "tracks") coat and process photoresists on wafers.

Semiconductors are products produced by the semiconductor industry. These products include chips, discretes, optoelectronics, and sensors. The term semiconductor is also separately used to refer to materials with electrical properties in between conductors and insulators.

Semiconductor manufacturing equipment includes tools used to fabricate, assemble, test, and package chips.

Testing ensures fabricated chips operate as intended.

Wafers are thin, disc-shaped materials in which chips are fabricated.

Wafer bonders and aligners join silicon wafers, often after chips are fabricated in the wafers.

Wafer and photomask handlers store and transport wafers and photomasks in a fab.

Wafer marking systems mark wafers or chips manufactured in wafers with identifiers using a laser.

Wet chemicals are materials used in semiconductor fabrication.

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Endnotes

[1] Saif M. Khan, "U.S. Semiconductor Exports to China: Current Policies and Trends" (Washington, DC: Center for Security and Emerging Technology, October 2020), https://cset.georgetown.edu/wp-content/uploads/U.S.-Semiconductor-Exports-to-China-Current-Policies-and-Trends.pdf.

[2] Saif M. Khan, "Securing Semiconductor Supply Chains" (Washington, DC: Center for Security and Emerging Technology, January 2021).

[3] Will Hunt, Saif M. Khan, and Dahlia Peterson, "China's Progress in Semiconductor Manufacturing Equipment: Accelerants and Policy Implications" (Washington, DC: Center for Security and Emerging Technology, Forthcoming, 2021).

[4] Semiconductors include several categories. The most important category is computer chips, which include logic chips, memory chips, and analog chips. Others include optoelectronics, sensors, and discretes.

[5] Syed Alam, Timothy Chu, Shrikant Lohokare, Shungo Saito, and McKinley Baker, "Globality and Complexity of the Semiconductor Ecosystem" (Accenture and Global Semiconductor Alliance, 2020), https://www.accenture.com/_acnmedia/PDF-119/Accenture-Globality-Semiconductor-Industry.pdf.

[6] "Beyond Borders: The Global Semiconductor Value Chain" (San Jose, CA: Semiconductor Industry Association, May 2016), 6–7, https://www.semiconductors.org/wp-content/uploads/2018/06/SIA-Beyond-Borders-Report-FINAL-May-6-1.pdf.

[7] The specification step is a "high value-added function that applies the firm's market knowledge and [IP] in deciding what feature set and performance level will be most profitable." Clair Brown and Greg Linden, *Chips and Change: How Crisis Reshapes the Semiconductor Industry* (Cambridge, MA: MIT Press, August 19, 2011), 64.

[8] Brown et al., "Chips and Change," 67.

[9] Brown et al., "Chips and Change," 67.

[10] Core IP is heavily protected by patents, trade secrets, and control of standards to maintain competitive advantages. Brown et al., "Chips and Change," 159–160.

[11] These steps are respectively called front-end-of-line processing and back-end-of-line processing.

[12] For a basic description of these steps, see the series beginning with "Eight Major Steps to Semiconductor Fabrication, Part 1: Creating the Wafer," *Samsung Newsroom*, April 22, 2015, https://news.samsung.com/global/eight-major-steps-to-semiconductor-fabrication-

part-1-creating-the-wafer. For a full technical description of these steps' order and interplay, see Robert J. Lopes, "Semiconductor Processing," ECE 684: Advanced Microprocessor Systems, New Jersey Institute of Technology, Newark, NJ, https://web.njit.edu/~rlopes/Mod2.1.pdf.

[13] For chip end uses, see "2020 State of the U.S. Semiconductor Industry," (San Jose, CA: Semiconductor Industry Association, June 2020), 4–5, https://www.semiconductors.org/wp-content/uploads/2020/06/2020-SIA-State-of-the-Industry-Report.pdf. For AI chip end uses, see Gaurav Batra, Zach Jacobson, Siddarth Madhav, Andrea Queirolo, and Nick Santhanam, "Artificial-intelligence hardware: New opportunities for semiconductor companies" (McKinsey and Company, January 2019), Exhibit 4, https://www.mckinsey.com/industries/semiconductors/our-insights/artificial-intelligence-hardware-new-opportunities-for-semiconductor-companies.

[14] Market shares are from 2019, except ATP market shares, which are from 2018. IDMs perform a large percentage of design, fabrication, and ATP and do not separately report revenues for these activities. Therefore, the market shares for these three segments are based on CSET's estimates. ATP market shares and country- and region-level values sum to more than 100 percent due to rounding.

[15] For China's self-sufficiency in each sector, see Cheng Ting-Fang and Lauly Li, "How China's chip industry defied the coronavirus lockdown," *Nikkei Asia*, March 18, 2020, https://asia.nikkei.com/Spotlight/The-Big-Story/How-China-s-chip-industry-defied-the-coronavirus-lockdown.

[16] Items are more robust chokepoints if they are (1) tangible and difficult to steal or copy, (2) expensive, (3) dependent on talent requiring implicit know-how to produce, and (4) produced by a small number of suppliers, especially because of natural economic forces such as high capital barriers to entry and economies of scale.

[17] "Semiconductor R&D Spending Will Step Up After Slowing," *IC Insights*, January 31, 2019, https://www.icinsights.com/news/bulletins/Semiconductor-RD-Spending-Will-Step-Up-After-Slowing/.

[18] "2020 SIA Factbook" (San Jose, CA: Semiconductor Industry Association, 2020), 17, https://www.semiconductors.org/wp-content/uploads/2020/04/2020-SIA-Factbook-FINAL_reduced-size.pdf.

[19] "Top 10 Semiconductor R&D Spenders Increase Outlays 6% in 2017," *IC Insights*, February 16, 2018, https://www.icinsights.com/news/bulletins/Top-10-Semiconductor-RD-Spenders-Increase-Outlays-6-In-2017/.

[20] Bart van Hezewijk, "China Winning the Future of the semiconductor industry?", *SemiWiki.com*, September 1, 2019, https://semiwiki.com/general/274582-china-winning-the-future-of-the-semiconductor-industry/.

[21] OECD, *International Technology Transfer Policies* (Paris, France: OECD Trade Policy Papers, No. 222, OECD Publishing, January 24, 2019), 28, 42, https://doi.org/10.1787/7103eabf-en.

[22] "2019 SIA Factbook" (San Jose, CA: Semiconductor Industry Association, 2019), 3, https://www.semiconductors.org/wp-content/uploads/2019/05/2019-SIA-Factbook-FINAL.pdf; van Hezewijk, "China Winning the Future."

[23] Semiconductor Industry Association, "2020 Factbook," 20.

[24] There is some question as to whether public semiconductor R&D "crowds-in" (increases) or "crowds-out" (decreases) private semiconductor R&D. One study commissioned by the Semiconductor Industry Association suggests a "crowding-in" effect where public R&D spurs private R&D. "Sparking Innovation: How Federal Investment in Semiconductor R&D Spurs U.S. Economic Growth and Job Creation" (Arlington, VA: Nathan Associates, June 2020), https://www.semiconductors.org/wp-content/uploads/2020/06/SIA_Sparking-Innovation_Addendum_6.8.20.pdf.

[25] For a full breakdown of this spending by agency and project, see Nathan Associates, "Sparking Innovation."

[26] Michaela D. Platzer and John F. Sargent Jr., *U.S. Semiconductor Manufacturing: Industry Trends, Global Competition, Federal Policy* (Washington, DC: Congressional Research Service, June 27, 2016), 8, https://fas.org/sgp/crs/misc/R44544.pdf.

[27] "Measuring distortions in international markets: The semiconductor value chain" (Paris: Organisation for Economic Cooperation and Development, December 12, 2019), 62, 84, https://doi.org/10.1787/8fe4491d-en.

[28] In 2014, China began a plan to subsidize its semiconductor industry with $150 billion over 10 years. Yuan Gao, "China Is Raising Up to $31.5 Billion to Fuel Chip Vision," *Bloomberg*, March 1, 2018, https://www.bloomberg.com/news/articles/2018-03-01/china-is-said-raising-up-to-31-5-billion-to-fuel-chip-vision.

[29] OECD, "Measuring distortions," 84.

[30] "WSTS Semiconductor Market Forecast Spring 2020," World Semiconductor Trade Statistics, June 9, 2020, https://www.wsts.org/esraCMS/extension/media/f/WST/4622/WSTS_nr-2020_05.pdf; Semiconductor Industry Association, "2020 Factbook," 11. By comparison, estimates by IC Insights put 2019 semiconductor production at $444.5 billion. "McLean Report," IC Insights, accessed September 4, 2020, https://www.icinsights.com/services/mcclean-report/report-contents/; "O-S-D Report," IC Insights, accessed September 4, 2020, https://www.icinsights.com/services/osd-report/.

[31] Many factors drove vertical specialization and modularization. First, chip design businesses could compete without massive investments needed to build fabs. Second, chip design has become more specialized, so a relatively greater share of value is in design than in fab process knowledge compared to the 1970s. Third, standardization toward metal-oxide-semiconductor processes involving predictably uniform transistor density improvements allowed design firms to predict foundry capabilities from the outside. Fourth, the development of EDA software provided a standardized interface between fabless firms and foundries. Fifth, expansion of markets allowed vertically specialized firms to exploit economies of scale and specialization. Sixth, as chip performance—which IDMs optimize—have improved, they have become less of a bottleneck for customers as compared to flexibility—which the fabless-foundry model optimizes. Semiconductor Industry Association, "Beyond Borders," 7–8; Brown et al., "Chips and Change," 46; Ben Thompson, "Chips and Geopolitics," *Stratechery*, May 19, 2020, https://stratechery.com/2020/chips-and-geopolitics/. However, IDMs like Intel still benefit from closer feedback between design and fabrication for the development of less predictable, cutting-edge semiconductors. Additionally, memory chipmakers still operate exclusively according to the IDM model, given greater challenges in separating memory chip design and fabrication.

[32] For a list of the top fabless firms, see Peter Clarke, "US entity list hit fabless chip vendors in 2019," *eeNews Analog*, March 19, 2020, https://www.eenewsanalog.com/news/us-entity-list-hit-fabless-chip-vendors-2019. For a detailed analysis of China's fabless firms, see "Current Status of the Integrated Circuit Industry in China — IC Design Industry," *J. Microelectron. Manuf.*, Vol. 1, No. 1 (September 30, 2018), http://www.jommpublish.org/p/13/.

[33] Fabless firms sometimes outsource design work to "design service firms" that do some or all of the design work, but do not themselves market the designs. Douglas B. Fuller, *Paper Tigers, Hidden Dragons: Firms and the Political Economy of China's Technological Development* (Oxford: Oxford University Press, 2016), 115. Additionally, foundries sometimes perform ATP.

[34] For IDM vs. fabless shares, see IC Insights, "McLean Report." The IDM and fabless country shares from SIA. Foundry data is from CSET estimates and "U.S. IC Companies Maintain Global Marketshare Lead," *IC Insights*, March 29, 2020, https://www.icinsights.com/news/bulletins/US-IC-Companies-Maintain-Global-Marketshare-Lead/. The OSAT data is from "TOP 25 OSATs Ranking 2018," *anysilicon*, July 3, 2019, https://anysilicon.com/top-25-osats-ranking-2018/.

[35] Semiconductor Industry Association, "State of the U.S. Semiconductor Industry," 7–8; IC Insights, "U.S. IC Companies." The DRAM and NAND data is from TrendForce.

[36] The data for microprocessors, discrete GPU, FPGA, DRAM, and NAND from VLSI Research. These values do not precisely match the WSTS data in Figure 5.

[37] Eugenia Liu and Shanshan Du, "IC Design Leads China's IC Ecosystem Development," *SEMI*, November 1, 2018, https://blog.semi.org/business-markets/ic-design-leads-chinas-

ic-ecosystem-development; Paul Triolo and Graham Webster, "China's Efforts to Build the Semiconductors at AI's Core," *New America*, December 7, 2018, https://www.newamerica.org/cybersecurity-initiative/digichina/blog/chinas-efforts-to-build-the-semiconductors-at-ais-core/.

[38] "China IC Ecosystem Report" (Milpitas, CA: SEMI, 2017 edition), 18.

[39] "HiSilicon First China-Based Semi Supplier to be Ranked in Top-10," *IC Insights*, May 6, 2020, https://www.icinsights.com/news/bulletins/HiSilicon-First-ChinaBased-Semi-Supplier-To-Be-Ranked-In-Top10/. However, U.S. export controls that prevent Huawei from outsourcing fabrication to Taiwan-based TSMC could put that ranking in jeopardy. Khan, "U.S. Semiconductor Exports to China."

[40] "美国统治力惊人，中国半导体如何在炮火中匍匐前进? [U.S. dominance is amazing. How can Chinese semiconductors crawl forward under the gunfire?]," *eefocus*, November 21, 2018, https://www.eefocus.com/mcu-dsp/424622.

[41] Therefore, China achieves low self-sufficiency for a wide variety of logic chips. Liu Qianqian and Ma Haoran, "National Defense Informatization In-Depth Report Series—The Time to Replace Imports with Independently Controllable Domestically Produced Versions is Now [国防信息化深度系列报告——自主可控国产化替代时不我待]" (Pacific Securities (太平洋证券), April 2018), 16, http://pdf.dfcfw.com/pdf/H3_AP201804271132194582_1.pdf.

[42] As of 2019, the United States (55 firms), China (26 firms), Europe (12 firms), and other regions were selling or developing AI chips: GPUs, FPGAs, and AI ASICs. Daniel Castro, Michael McLaughlin and Eline Chivot, "Who Is Winning the AI Race: China, the EU or the United States?," *Center for Data Innovation*, August 19, 2019, https://www.datainnovation.org/2019/08/who-is-winning-the-ai-race-china-the-eu-or-the-united-states/.

[43] For Intel and AMD market data, see Paul Alcorn, "AMD vs. Intel CPU Market Share Q4 2019: EPYC and Desktop CPU Growth Decelerates, Mobile Ryzen Roars," *Tom's Hardware*, February 5, 2020, https://www.tomshardware.com/news/amd-vs-intel-cpu-market-share-q4-2019-epyc-and-ryzen-growth-decelerate-mobile-ryzen-up; "AMD vs Intel Market Share," CPU Benchmarks, accessed September 4, 2020, https://www.cpubenchmark.net/market_share.html. U.S., Taiwanese, and South Korean firms are the main producers of lower-end smartphone CPUs, often licensing U.K. core IP. "MediaTek lost glory as Qualcomm gained smartphone processor market share," *telecomlead*, May 29, 2018, https://www.telecomlead.com/telecom-statistics/mediatek-lost-glory-as-qualcomm-gained-smartphone-processor-market-share-84373.

[44] Zhiye Liu, "China's Latest Loongson CPUs Are On Par With AMD's Excavator," *Tom's Hardware*, December 26, 2019, https://www.tomshardware.com/news/loongson-cpus-catching-amd.

[45] Chen Qingqing, "High-tech de-Americanization accelerated," *Global Times*, December 25, 2019, https://www.globaltimes.cn/content/1174804.shtml.

[46] Kate O'Keefe and Brian Spegele, "How a Big U.S. Chip Maker Gave China the 'Keys to the Kingdom,'" *Wall Street Journal*, June 27, 2019, https://www.wsj.com/articles/u-s-tried-to-stop-china-acquiring-worldclass-chips-china-got-them-anyway-11561646798.

[47] Paul Alcorn, "Zhaoxin KaiXian x86 CPU Tested: The Rise of China's Chips," *Tom's Hardware*, April 10, 2020, https://www.tomshardware.com/features/zhaoxin-kx-u6780a-x86-cpu-tested.

[48] For a list of nodes, see "Technology Node," Wikichip, accessed September 4, 2020, https://en.wikichip.org/wiki/technology_node.

[49] Saif M. Khan and Alexander Mann, "AI Chips: What They Are and Why They Matter" (Washington, DC: Center for Security and Emerging Technology, April 2020), https://cset.georgetown.edu/research/ai-chips-what-they-are-and-why-they-matter, 24–25.

[50] eefocus, "[U.S. dominance is amazing]."

[51] He Huifeng, "Beijing did a tech reality check on its industrial champions. The results were not amazing," *South China Morning Post*, July 18, 2018, https://www.scmp.com/news/china/economy/article/2155862/beijing-did-tech-reality-check-its-industrial-champions-results.

[52] Dario Amodei and Danny Hernandez, "AI and Compute," *OpenAI*, May 16, 2018, https://openai.com/blog/ai-and-compute/.

[53] Hassan Mujtaba, "AMD Radeon GPUs Gained Big Chunk Of Discrete Market Share Versus NVIDIA GeForce In Q4 2019 – Up From 27% To 31%," *Wccftech*, March 5, 2020, https://wccftech.com/amd-radeon-and-nvidia-geforce-discrete-gpu-market-share-q4-2019/.

[54] Intel also produces less powerful GPUs for inclusion in systems-on-chips. Jon Peddie & Robert Dow, "Continued growth in total global GPU shipments in Q4'19 reports Jon Peddie Research," *Jon Peddie Research*, February 24, 2020, https://www.jonpeddie.com/press-releases/continued-growth-in-total-global-gpu-shipments-in-q419-reports-jon-peddie-r. It is also attempting to enter the discrete GPU market, though its planned chip is low end and unlikely to be competitive with Nvidia and AMD's discrete GPUs. Sean Hollister, "This is Intel's first discrete graphics card in 20 years, but you can't buy one," *The Verge*, January 9,

2020, https://www.theverge.com/2020/1/9/21058422/intel-dg1-discrete-gpu-graphics-card-announcement-ces-2020.

[55] "China-made GPUs make substantial progress," *cnTechPost*, May 12, 2020, https://cntechpost.com/2020/05/12/china-made-gpus-make-substantial-progress/.

[56] Zhiye Liu, "Chinese Vendor Developing PCIe 4.0 GPU With 16GB HBM and GTX 1080-Like Performance," *Tom's Hardware*, August 22, 2019, https://www.tomshardware.com/news/jingjia-micro-chinese-gpu-pcie-4.0-16gb-hbm-gtx-1080-performance,40217.html.

[57] Paul Dillien, "And the Winner of Best FPGA of 2016 is...," *EE Times*, March 6, 2017, https://web.archive.org/web/20181008063015/https://www.eetimes.com/author.asp?doc_id=1331443; "List of FPGA Companies," *HardwareBee*, August 4, 2018, https://hardwarebee.com/list-fpga-companies/.

[58] Khan et al., "AI Chips," 28.

[59] "Efinix® Partners with Samsung to Develop Quantum™ eFPGAs on 10nm Silicon Process," *Efinix*, May 8, 2019, https://www.efinixinc.com/company-pr-efinix-partners-with-samsung-for-10nm.html.

[60] Khan et al., "AI Chips," 20–23.

[61] Walden C. Rhines, "Electronic Design Evolution," National Academy of Sciences meeting, February 11, 2020, 11.

[62] This is because design engineers need to optimize ASICs for a single or narrower use cases rather than many unforeseeable use cases as with CPUs, GPUs, and FPGAs. Khan et al., "AI Chips," 28–31.

[63] For benchmarks relative to leading firms, see "MLPerf Training v0.7 Results," *MLPerf*, July 29, 2020, https://mlperf.org/training-results-0-7.

[64] VLSI Research. Other segments include SRAM, EPROM, MASK ROM, and NOR flash.

[65] Cheng Ting-Fang and Laury Li, "China memory chip output zooms from zero to 5% of world total," *Nikkei Asia*, November 20, 2019, https://asia.nikkei.com/Business/China-tech/China-memory-chip-output-zooms-from-zero-to-5-of-world-total; see also Eliza Gkritsi, "A Chinese firm made a memory chip that can compete with Samsung. What's next?," *TechNode*, April 23, 2020, https://technode.com/2020/04/23/ymtc-memory-chip/.

[66] "Without Technology, China's "MIC 2025" Results for ICs Likely to Fall Woefully Short of its Goals," *IC Insights*, January 31, 2017,

https://www.icinsights.com/news/bulletins/Without-Technology-Chinas-MIC-2025-Results-For-ICs-Likely-To-Fall-Woefully-Short-Of-Its-Goals/.

[67] Cheng Ting-Fang, "China's top memory chipmaker to unveil first-ever storage products," *Nikkei Asia*, June 28, 2020, https://asia.nikkei.com/Business/China-tech/China-s-top-memory-chipmaker-to-unveil-first-ever-storage-products.

[68] For a detailed analysis of China's memory chipmakers, see "Current Status of the Integrated Circuit Industry in China — Overview of the Memory Industry," *J. Microelectron. Manuf.*, Vol. 3, No. 2 (June 29, 2020), http://www.jommpublish.org/p/53/.

[69] OECD, "Measuring distortions," 84.

[70] Dan Kim and John VerWey, "The Potential Impacts of the Made in China 2025 Roadmap on the Integrated Circuit Industries in the U.S., EU and Japan," (Washington, DC: U.S. International Trade Commission, August 2019), 7–8, https://www.usitc.gov/publications/332/working_papers/id_19_061_china_integrated_circuits_technology_roadmap_final_080519_kim_verwey-508_compliant.pdf. In 2017, half of the top 10 chipmakers in China were foreign. SEMI, "China IC Ecosystem," 20.

[71] IC Insights, "U.S. IC Companies." Totals are CSET estimates based on a weighted average of chip IDM country shares, OSD IDM country shares (using SEMI fab capacity shares as a proxy, weighting optoelectronics, sensors, and discretes according to WSTS market statistics), and foundry country shares. For the weightings, we assume chip IDMs, OSD IDMs, and foundries respectively have 53.0, 19.5, and 27.5 percent fab market shares, calculated as follows. In 2019, chip IDMs, OSD IDMs, and foundries respectively generated 57.2, 19.5, and 23.4 percent of semiconductor sales. IC Insights, "McLean Report"; IC Insights, "O-S-D Report." However, chip IDM purchases generated 15 percent of foundry revenue in 2019, reducing IDM fab market share to 53.0 percent and increasing foundry market share to 27.5 percent. IC Insights; Rhines, "Electronic Design Evolution," 24.

[72] The data includes 200 mm-equivalent wafer capacity for all fabs operating at the end of 2020. For Figures 10 and 11, there are several acknowledged limitations in the way we estimate wafer fab capacity. First, in cases where a fab is owned by two firms headquartered in different countries, we allocate its fab capacity equally between the co-owners. Second, many fabs process different nodes, so not all of their capacity is at the smallest node they support. Because it is difficult to get the specific breakdown of capacity by node in a single fab, for the "logic ≤45 nm" category in Figures 10 and 11, we included 100% of a fab's capacity as long as it supports or is planned to support any amount of capacity at a ≤45 nm node.

[73] The fab type categories exclude small amounts of fab shares for foundries producing memory chips. analog chips, sensors, and chips using epitaxial wafers.

[74] Because only IDMs produce memory chips, the same memory chip designers mentioned in the "design" subsection hold memory chip fab capacity, which approximately maps to

memory chip design market shares. However, China's memory fab shares in Figures 10 and 11 and Table 5 are much higher than their market shares in the "design" subsection because some of that fab capacity is aspirational and planned to begin operation in the near future.

[75] Belgium hosts Interuniversity Microelectronics Centre, an international R&D hub that runs an R&D fab with advanced logic capacity. But it is not used for volume manufacturing.

[76] "Foundry Revenue Estimated to Grow by 30% YoY in 1Q20, while COVID-19 Pandemic May Hinder Future Market Demand, Says TrendForce," *TrendForce*, March 19, 2020, https://www.trendforce.com/presscenter/news/20200319-10246.html; "Leading-Edge Leads the Way in Pure-Play Foundry Growth," *IC Insights*, September 28, 2016, http://www.icinsights.com/news/bulletins/LeadingEdge-Leads-The-Way-In-PurePlay-Foundry-Growth/.

[77] "Revenue per Wafer Rising As Demand Grows for sub-7nm IC Processes," *IC Insights*, February 20, 2020, https://www.icinsights.com/news/bulletins/Revenue-Per-Wafer-Rising-As-Demand-Grows-For-Sub7nm-IC-Processes/.

[78] Arne Verheyde, "Taiwan Semiconductor Manufacturing Company Losing Its Process Leadership To Intel," *Seeking Alpha*, April 21, 2020, https://seekingalpha.com/article/4338843-taiwan-semiconductor-manufacturing-company-losing-process-leadership-to-intel.

[79] Ian King, "Intel Plunges as It Weighs Exit From Manufacturing Chips," *Bloomberg*, July 23, 2020, https://www.bloomberg.com/news/articles/2020-07-24/intel-considers-what-was-once-heresy-not-manufacturing-chips.

[80] SEMI, "China IC Ecosystem," 14.

[81] "World Fab Forecast" (Milpitas, CA: SEMI, November 2020 edition); Wei Shang, "SMIC to the rescue? Huawei shouldn't hold its breath: experts," *TechNode*, May 22, 2020, https://technode.com/2020/05/22/smic-to-the-rescue-huawei-shouldnt-hold-its-breath-experts/.

[82] David Manners, "Hua Hong heads for 5nm," *Electronics Weekly*, February 27, 2019, https://www.electronicsweekly.com/news/business/hua-hong-heads-5nm-2019-02/. In 2020, Chinese chipmaker HSMC—which recruited engineers from TSMC—tried to develop 7 nm capacity but failed due to lack of funding. Wei Sheng, "HSMC promised China's first 7 nm chips. It didn't go well," *TechNode*, September 9, 2020, https://technode.com/2020/09/09/hsmc-promised-chinaa-first-7-nm-chips-it-didnt-go-well/.

[83] Khan et al., "AI Chips," 12.

[84] Khan, "U.S. Semiconductor Exports to China."

[85] Fuller, *Paper Tigers*, 114.

[86] SEMI, "China IC Ecosystem," 27.

[87] Semiconductor Industry Association, "Proposed Determination of Action Pursuant to Section 301: China's Acts, Policies, and Practices Related to Technology Transfer, Intellectual Property, and Innovation," USTR-2018-0018, July 28, 2018, 7, https://www.semiconductors.org/wp-content/uploads/2018/08/Final-_SIA_Submission_on_301_Tariffs.pdf.

[88] Joel Hruska, "TSMC to Build Supercomputing AI Chips, Ramps Wafer-Scale Computing," *ExtremeTech*, July 6, 2020, https://www.extremetech.com/computing/312392-tsmc-to-build-supercomputing-ai-chips-ramps-wafer-scale-computing.

[89] H.-S. Philip Wong et al., "A Density Metric for Semiconductor Technology," *IEEE*, Vol. 8, No. 4 (April 2020): 480, https://ieeexplore.ieee.org/document/9063714.

[90] Moore's Law is the historical observation that transistor density has doubled every two years.

[91] For a summary of advanced packaging techniques and challenges, see Mark LaPedus, "The Race To Much More Advanced Packaging," *Semiconductor Engineering,* July 23, 2020, https://semiengineering.com/the-race-to-much-more-advanced-packages/; Mark LaPedus, "Packaging Biz Faces Challenges In 2019," *Semiconductor Engineering,* December 10, 2018, https://semiengineering.com/packaging-biz-faces-challenges-in-2019/. For market sizes of advanced packaging segments, see "Advanced packaging: OSATs, foundries, and IDMs all want to be part of the game," *Yole Développement*, 2020, http://www.yole.fr/AdvancedPackaging_Industry_Update_SYNAPS.aspx.

[92] anysilicon, "TOP 25 OSATs." OSAT market size is based on the top 25 OSAT vendors. "Press Releases Gallery - Advanced Packaging," Yole Développement, accessed September 4, 2020, http://www.yole.fr/2014-galery-3D.aspx/. Although some foundries like TSMC do some ATP, we assume all non-OSAT ATP is done by IDMs for the purposes of our calculations.

[93] We estimate IDM and foundry ATP market size based on Gartner's estimate that OSATs control 53 percent of the ATP market. Mark LaPedus, "OSAT Biz: Growth And Challenges," *Semiconductor Engineering*, February 8, 2017, https://semiengineering.com/osat-biz-growth-and-challenges/; Jim Walker, "Semiconductor Road Conditions: Slow, Bumpy, But Straight Ahead," *Gartner*, September 15, 2015, http://meptec.org/Resources/Sept%202015%20Gartner%20Luncheon%20Presentation.pdf.

[94] Aside from the SME survey in this section, others have also identified key Chinese SME firms and research institutes. Lily Feng and Dan Tracy, "Domestic Equipment Suppliers in China Seek Both Semiconductor and Solar Industry Growth," SEMI, accessed September 4,

2020, https://www.semi.org/en/P044326; For a comprehensive treatment of Chinese SME firms, but less comprehensive treatment to Chinese research institutes, see "Current Status of the Integrated Circuit Industry in China — IC Special Equipment Industry," *J. Microelectron. Manuf.*, Vol. 2, No. 1 (March 29, 2019): 6, http://www.jommpublish.org/p/26/.

[95] Chinese SME firms struggle to supply even the Chinese market—in 2017, they captured only 5 percent of the Chinese market. SEMI, "China IC Ecosystem," 35.

[96] Khan, "Securing Semiconductor Supply Chains."

[97] Hunt et al., "China's Progress in Semiconductor Manufacturing Equipment."

[98] The furnace forms a cylindrical ingot of silicon from polycrystalline raw silicon. The machining equipment cuts the ingot into wafers used for chip fabrication.

[99] Four small Chinese firms and research institutes produce some versions of these tools. Feng et al., "Domestic Equipment Suppliers.

[100] "Wafer Aligner/Bonder —— IC Back-end Manufacturing," SMEE, accessed September 4, 2020, http://www.smee.com.cn/eis.pub?service=homepageService&method=indexinfo&onclicknodeno=1_4_1_5.

[101] Ion implanters have several components. An ion source, such as a gas, contains dopants. An ion accelerator applies an electric field to transfer a beam of ions from the gas to the silicon wafer. To ensure the ion beam does not contain contaminants, a mass spectrometer separates undesired particles from the beam. A beam sweeper is used to scan the ion beam over different parts of the wafer. For more on ion implanter technology, see Chris A. Mack, "Lecture 16: Ion Implantation, part 1," CHE323/CHE384: Chemical Processes for Micro- and Nanofabrication, University of Texas, Austin, TX, 2013, http://www.lithoguru.com/scientist/CHE323/Lecture16.pdf.

[102] For key uses cases in semiconductor fabrication, see Mack, "Ion Implantation."

[103] "CETC, an active player in the Belt and Road (B&R) Initiative," CETC, accessed September 4, 2020, http://cetcsolarenergy.com/b&r/ion_implanter.html.

[104] "China delivers first CMP equipment for use in integrated circuit manufacturing," *China Knowledge*, June 20, 2018, https://www.chinaknowledge.com/News/DetailNews?id=67955.

[105] SEMI, "China IC Ecosystem," 36; Zhao Zhuqing, "高能离子注入机：我国芯片制造核心关键装备再获突破 [High-energy ion implanter: my country's core key equipment for chip

manufacturing achieves another breakthrough]," *People's Daily Online*, July 1, 2020, http://scitech.people.com.cn/n1/2020/0701/c1007-31766302.html.

[106] "iPV-3000," Kingstone Semiconductor, accessed September 4, 2020, http://www.kingstonesemi.com/en/product/154.html.

[107] The ion beam lithography market is minimal for chip and mask making, but has a $820 million market overall. "Focused Ion Beam Market," *Markets and Markets*, November 2019, https://www.marketsandmarkets.com/Market-Reports/focused-ion-beam-market-20057108.html. However, it can potentially be used for both.

[108] Robert Castellano, "Canon's Nanoimprint Lithography: A Chink In ASML Holding's Armor", *Seeking Alpha*, March 19, 2019, https://seekingalpha.com/article/4249762-canons-nanoimprint-lithography-chink-asml-holdings-armor; "MA300 Gen2 Mask Aligner," SÜSS MicroTec, accessed September 4, 2020, https://www.suss.com/en/products-solutions/mask-aligner/ma300-gen2; Vu Luong, "EUV Lithography Coming to your local IC manufacturer! Soon," *Interuniversity Microelectronics Centre*, May 16, 2018, 13, https://eng.kuleuven.be/en/research/phd/arenberg-youngster-seminars/ays-pdf/20180516-luong-ays-final.pdf. ASML is developing more advanced EUV tools for the 3 nm node. Mark LaPedus, "Multi-Patterning EUV Vs. High-NA EUV," *Semiconductor Engineering*, December 4, 2019, https://semiengineering.com/multi-patterning-euv-vs-high-na-euv/.

[109] Scanners and steppers operate as follows. They each have a light source that produces ultraviolet light at the various wavelengths shown in Table 10. The tool refracts the light and passes it through a photomask—a transparent plate with a circuit pattern—to transfer that pattern to a chemical called a photoresist applied as a layer on the chip. The light dissolves parts of the photoresist in the circuit pattern. The newly created photoresist pattern is etched into a permanent chip substrate below the photoresist, then the photoresist is removed. A stepper "steps" the wafer between different locations, while keeping the photomask in the same position, so that the photomask pattern can be transferred to different locations of the wafer. A scanner goes further and moves both the wafer and the photomask.

[110] ASML sells a single EUV scanner for about $123 million. Khan et al., "AI Chips," 12. A 5 nm fab requires multiple EUV scanners.

[111] Photolithography costs have diverged upward from non-photolithography costs since the 16 nm node. Photolithography tool cost remained constant per unit wafer area up to at least 2012 because of increasing yields (i.e. the percentage of chips without manufacturing errors), equipment productivity, and wafer sizes. The last wafer size increase to 300 mm occurred in 2002. Larger wafers increase relative photolithography costs, to the point where 50 percent of 300 mm wafer processing costs are for photolithography compared to 25 percent for 150 mm wafers. Chris A. Mack, "Lecture 3: Semiconductor Economics," CHE323/CHE384: Chemical Processes for Micro- and Nanofabrication, University of Texas, Austin, TX, 2013, http://lithoguru.com/scientist/CHE323/Lecture3.pdf. For example, larger wafers reduce non-lithography costs by reducing the number of times

deposition, etch, and other steps must be performed. Scotten W. Jones, "Technology and Cost Trends at Advanced Nodes," *IC Knowledge LLC*, accessed September 4, 2020, 9, https://www.icknowledge.com/news/Technology%20and%20Cost%20Trends%20at%20Advanced%20Nodes%20-%20Revised.pdf.

[112] One EUV scanner also weighs about 180,000 kilograms, and ships in 40 freight containers. "A backgrounder on Extreme Ultraviolet (EUV) lithography," *ASML*, January 18, 2017, https://medium.com/@ASMLcompany/a-backgrounder-on-extreme-ultraviolet-euv-lithography-a5fccb8e99f4. Given its complexity, ASML has had difficulty manufacturing EUV scanners at a pace meeting demand. ASML's EUV order backlog is approaching two years. David Schor, "ASML Q4: NXE:3400C Machines Ramp; Strong Growth Due to EUV in 2020," *WikiChip Fuse*, January 22, 2020, https://fuse.wikichip.org/news/3250/asml-q4-nxe3400c-machines-ramp-strong-growth-due-to-euv-in-2020/.

[113] ASML (Netherlands) controls over 85 percent of the market for scanners and steppers, while Nikon (Japan) and Canon (Japan) capture virtually all of the rest. Robert Castellano, "ASML: My Top Semiconductor Processing Equipment Company Pick," *Seeking Alpha*, January 27, 2020, https://seekingalpha.com/article/4319159-asml-top-semiconductor-processing-equipment-company-pick. For photolithography market share by unit sales over time, see Anton Shilov, "ASML, Carl Zeiss, and Nikon to Settle Legal Disputes Over Immersion Lithography," *AnandTech*, January 25, 2019, https://www.anandtech.com/show/13901/asml-carl-zeiss-and-nikon-to-settle-legal-disputes-over-immersion-lithography. Only ASML and Nikon sell photolithography tools used at scale for ≤90 nm nodes, and only ASML for 5 nm. For the number of photolithography firms operating at each node when that node was introduced, see Khan et al., "AI Chips," 12. No other major SME sectors exhibit this degree of consolidation.

[114] ASML has a 17 percent SME market share and 97 percent of its business is scanners and steppers, while leading U.S. SME firms Applied Materials, Lam Research, and KLA collectively have a 36 percent SME market share and sell a wide variety of SME, focusing on deposition, etch, and process control tools. Yet as of trading close on November 9, 2020, ASML's market capitalization was $171 billion while the others' were collectively $161 billion. ASML's price/earnings (P/E) ratio was 43, while the other three had P/E ratios of respectively 21, 24, and 28, reflecting a market expectation of much larger future profits for photolithography tools than for other SME. In part, the market is predicting that no firms will break ASML's monopoly on EUV scanners, so ASML will reap monopoly profits on a highly-demanded, linchpin technology. Nikon and Canon, the next most advanced photolithography firms, are not trying to develop EUV technology. "How ASML became chipmaking's biggest monopoly," *The Economist*, February 29, 2020, https://www.economist.com/business/2020/02/29/how-asml-became-chipmakings-biggest-monopoly.

[115] EUV photolithography may no longer require multiple deposition and etch steps. Robert Castellano, "The Switch To ASML's EUV Lithography Will Impact The Entire Semiconductor Supply Chain," *Seeking Alpha*, March 30, 2017, https://seekingalpha.com/article/4059013-switch-asmls-euv-lithography-will-impact-

entire-semiconductor-supply-chain; Scotten Jones, "ISS 2018 – The Impact of EUV on the Semiconductor Supply Chain," *SemiWiki*, January 18, 2018, https://semiwiki.com/semiconductor-manufacturers/intel/7249-iss-2018-the-impact-of-euv-on-the-semiconductor-supply-chain/.

[116] According to the "remainder principle," "as technology reduces cost or increases performance on one task in a process or one component in a product, the value of performance on the remaining tasks or components increases," thereby increasing the need for skill and improvement on the remaining tasks. James Bessen, *Learning by Doing: The Real Connection Between Innovation, Wages, and Wealth* (New Haven, CT: Yale University Press, April 28, 2015), 44–48.

[117] Hassan N. Khan, David A. Hounshell, and Erica R. H. Fuchs, "Science and research policy at the end of Moore's law," *Nature Electronics*, Vol. 1, No. 1 (January 8, 2018), https://www.nature.com/articles/s41928-017-0005-9. They acquired 23 percent ownership of ASML for about €4 billion and committed an additional €1.5 billion to ASML for R&D. Ed Lin, "Intel Follows Samsung, Slashes Stake in ASML," *Barrons*, September 15, 2017, https://www.barrons.com/articles/intel-follows-samsung-slashes-stake-in-asml-1505476889.

[118] "First China-made 28nm lithography machine expected to be delivered in 2021-2022," *cnTechPost*, June 5, 2020, https://cntechpost.com/2020/06/05/first-china-made-28nm-lithography-machine-expected-to-be-delivered-in-2021-2022/; "600 Series Stepper —— IC Front-end Manufacturing," SMEE, accessed September 4, 2020, http://www.smee.com.cn/eis.pub?service=homepageService&method=indexinfo&onclicknodeno=1_4_4_1.

[119] ASML's EUV technology became viable for mass chip production a decade after ASML sold its first EUV tool.

[120] SMEE purportedly has an 80 percent market share in China's domestic packaging market. "中国半导体设备现在的状态到底是怎么样的 [What is the current state of China's semiconductor equipment?]," *elecfans*, January 21, 2020, http://m.elecfans.com/article/1153039.html.

[121] Robert Castellano, "Lithography For Advanced Packaging Equipment," *SemiWiki*, June 24, 2019, https://semiwiki.com/semiconductor-services/273023-lithography-for-advanced-packaging-equipment/.

[122] Zhang Yangfei and Zhang Zhihao, "New machine raises country's image in photolithography," *China Daily*, November 30, 2018, https://www.chinadaily.com.cn/a/201811/30/WS5c006df2a310eff30328be90.html.

[123] Mark LaPedus, "China Speeds Up Advanced Chip Development," *Semiconductor Engineering*, June 22, 2020, https://semiengineering.com/china-speeds-up-advanced-chip-development/.

[124] SÜSS MicroTec, "MA300 Gen2 Mask Aligner."

[125] An electron source fires an electron beam, which passes through electrostatic plates that orient the beam toward particular locations of a substrate.

[126] "VSB-Technology," Vistec, accessed September 4, 2020, https://www.vistec-semi.com/en/products-and-services/vsb-technology/; "EB Mask Writer EBM-9500," NuFlare, accessed September 4, 2020, http://www.nuflare.co.jp/english/products/beam/.

[127] Mark LaPedus, "What Happened To Nanoimprint Litho?," *Semiconductor Engineering*, March 19, 2018, https://semiengineering.com/what-happened-to-nanoimprint-litho.

[128] "A New Life for Nano-Imprint Lithography," *Novus Light*, December 24, 2019, https://www.novuslight.com/a-new-life-for-nano-imprint-lithography_N9932.html.

[129] South Korean SEMES makes KrF and other tracks, but not EUV or ArF immersion tracks. "Semiconductor Equipment," SEMES, accessed September 4, 2020, https://www.semes.com/product.do?ar_action=listProduct&sch_product_group=SC&ar_lang=EN. Germany's SUSS MicroTec does not advertise any advanced EUV or ArF immersion capabilities for its tracks. "Spin Coater, Spray Coater, Developer," SÜSS MicroTec, September 4, 2020, https://www.suss.com/en/products-solutions/coater-and-developer.

[130] SEMI, "China IC Ecosystem"; Xinglong Chen, "FEOL photo track technology: latest trends and development," *Kingsemi*, February 2018, 6–7, http://www.semiconchina.org/Semicon_China_Manager/upload/kindeditor/file/20180320/20180320111359_378.pdf.

[131] "KS-FT200/300 200/300mm coater & developer for IC manufacturing," Kingsemi, accessed September 4, 2020, http://en.kingsemi.com/?p=537&a=view&r=534&city_name=.

[132] Applied Materials alone captures half of global CVD market share. John VerWey, "The Health and Competitiveness of the U.S. Semiconductor Manufacturing Equipment Industry," *Office of Industries and Office of Economics of the U.S. International Trade Commission*, 5, July 2019, https://www.usitc.gov/publications/332/working_papers/id_058_the_health_and_competitiveness_of_the_sme_industry_final_070219checked.pdf.

[133] Plasma CVD is suitable for materials requiring low temperatures during deposition. LPCVD is commonly used to deposit polysilicon, tungsten, titanium, titanium nitride. HTCVD is used to deposit epitaxial layers.

[134] For example, ALD is used to create fine structures in FinFETs, which are the predominant transistor structure used in leading-edge chips. Dennis Hausmann, "How Atomic Layer Deposition Works," *Semiconductor Engineering*, March 15, 2018, https://semiengineering.com/a-look-at-atomic-layer-deposition-2/.

[135] "PECVD Series," Piotech, accessed September 4, 2020, http://en.sypiotech.cn/?p=478.

[136] "CVD Coating Equipment," Sky Technology Development, accessed September 4, 2020, http://www.sky.ac.cn/html/en/index.php?ac=article&at=list&tid=184.

[137] "Chemical Vapor Deposition Equipment," NAURA, accessed September 4, 2020, http://www.naura.com/en/index.php/product/product_list_all/844.html.

[138] Piotech, "PECVD Series"; "Atomic Layer Deposition Equipment," NAURA, accessed September 4, 2020, http://www.naura.com/en/index.php/product/product_list_all/1757.html.

[139] "Physical Vapor Deposition Equipment," NAURA, accessed September 4, 2020, http://www.naura.com/en/index.php/product/product_list_all/843.html.

[140] "PVD Coating Equipment," Sky Technology Development, accessed September 4, 2020, http://www.sky.ac.cn/html/en/index.php?ac=article&at=list&tid=183.

[141] There are three main categories of changes. First, RTP activates materials (such as dopants in transistors) to change their properties, modifies materials, or makes deposited films denser to improve their properties. "What is Rapid Thermal Processing," Applied Materials, accessed September 4, 2020, http://www.appliedmaterials.com/what-rapid-thermal-processing; "Rapid Thermal Processing," Applied Materials, accessed September 4, 2020, http://www.appliedmaterials.com/en-in/semiconductor/products/rapid-thermal-processing/info.

[142] "Diffusion Furnace Heating Elements for Semiconductor Processing," Thermcraft, accessed September 4, 2020, https://thermcraftinc.com/diffusion-furnace-heating-elements-semiconductor-processing/.

[143] "Oxide/Diff," NAURA, accessed September 4, 2020, http://www.naura.com/en/index.php/product/product_list_all/842.html.

[144] Spin-coating is most typically used to deposit "low-k inter-metal-dielectrics," which are insulators between metal interconnects in chips.

[145] "Coater," Kingsemi, accessed September 4, 2020, http://en.kingsemi.com/?p=537.

[146] These tools use electrolysis to deposit materials.

[147] AMEC mkes metalorganic chemical vapor deposition (MOCVD), which is used especially often for optoelectronics. "Prismo D-BLUE," AMEC, accessed September 4, 2020, https://www.amec-inc.com/productDetails.html?id=5d23ad45c13b9476e09bae1b.

[148] "Etch," Applied Materials, accessed September 4, 2020, http://www.appliedmaterials.com/semiconductor/products/etch/info.

[149] U.S.-based Lam Research alone captures 60 percent of global market share in etching tools. VerWey, "U.S. Semiconductor Manufacturing Equipment," 5.

[150] Major types of conductor and dielectric dry etching tools include sputter etching and plasma etching. Subtypes of plasma etching include reactive ion etching and deep reactive ion etching (a form of reactive ion etching used to make deep wells). The most commonly used form is reactive ion etching. Keren J. Kanarika et al., "Overview of atomic layer etching in the semiconductor industry," *Journal of Vacuum Science & Technology A*, Vol. 33, No. 2 020802 (March 5, 2015), https://avs.scitation.org/doi/10.1116/1.4913379.

[151] This capability is known as "anisotropic" etching.

[152] "Etch Products," Lam Research, accessed September 4, 2020, https://www.lamresearch.com/products/our-processes/etch/; Mark LaPedus, "Atomic Layer Etch Finally Emerges," *Semiconductor Engineering*, May 15, 2014, https://semiengineering.com/atomic-layer-etch-finally-emerges/; Keren J. Kanarik, Samantha Tan, and Richard A. Gottscho, "Atomic Layer Etching: Rethinking the Art of Etch," *J. Phys. Chem. Lett.* Vol. 9, No. 16 (August 10, 2018): 4814−4821, https://pubs.acs.org/doi/abs/10.1021/acs.jpclett.8b00997; Mark LaPedus, "Atomic Layer Etch Expands To New Markets," *Semiconductor Engineering*, July 16, 2020, https://semiengineering.com/atomic-layer-etch-expands-to-new-markets/.

[153] These firms include Applied Materials (U.S.), Lam Research (U.S.), Tokyo Electron (Japan), Hitachi (Japan), Corial (French subsidiary of U.S.-based Plasma Therm), and Oxford Instruments (U.K.). "Atomic Layer Etch (ALE)," Semiconductor Engineering, accessed September 4, 2020, https://semiengineering.com/knowledge_centers/manufacturing/process/atomic-layer-etch/; LaPedus, "Atomic Layer Etch Expands."

[154] LaPedus, "Atomic Layer Etch Expands."

[155] Lena Li and Jessie Shen, "AMEC 5nm plasma etching tools verified by TSMC," *DigiTimes*, December 21, 2018, https://www.digitimes.com/news/a20181221PD207.html; "专家：国产刻蚀机很棒，但只是造芯片的'配角' [Expert: The domestic etching machine is

great, but it is only a 'supporting role' for making chips]," *Science and Technology Daily*, February 13, 2019, https://www.guancha.cn/industry-science/2019_02_13_489932.shtml. AMEC was accordingly the first Chinese SME firm to be ranked in a customer satisfaction survey by market research firm VLSI Research. "AMEC first Chinese firm to be ranked in VLSIresearch's Customer Satisfaction Survey," *Semiconductor Today*, May 21, 2018, http://www.semiconductor-today.com/news_items/2018/may/amec_210518.shtml.

[156] At least for packaging, China has almost completely localized its use of etching tools, especially AMEC's tools. *elecfans*, "China's semiconductor equipment."

[157] "Plasma Etching Equipment," AMEC, accessed December 14, 2020, http://www.naura.com/en/index.php/product/product_list_all/907.html.

[158] Wassenaar Arrangement 2015 Plenary Agreements Implementation, Removal of Foreign National Review Requirements, and Information Security Updates, 81 Fed. Reg. 64,655 (September 20, 2016) (revising 15 CFR § 730, 734, 738, 740, 742, 743, 748, 770, 772, and 774. https://www.federalregister.gov/documents/2016/09/20/2016-21544/wassenaar-arrangement-2015-plenary-agreements-implementation-removal-of-foreign-national-review.

[159] AMEC's most advanced etching tools are deep reactive ion etching tools, less precise than atomic layer etching tools. "Etching equipment," AMEC, accessed September 4, 2020, https://www.amec-inc.com/products.html#Etch.

[160] "Stripper," Kingsemi, accessed September 4, 2020, http://en.kingsemi.com/?p=540; "KS-S300-E Single-wafer etcher," Kingsemi, accessed September 4, 2020, http://en.kingsemi.com/?p=541&a=view&r=544.

[161] "Cleaning Tool," NAURA, accessed September 4, 2020, http://www.naura.com/en/index.php/product/product_list_all/841.html.

[162] A rotating polishing pad (on which a reactive slurry is coated) is pressed against the wafer to flatten and polish it.

[163] "Universal-300 Dual," Hwatsing, accessed September 4, 2020, http://www.hwatsing.com/chanpinyufuwu/160-universal-300-dual; SEMI, "China IC Ecosystem," 36.

[164] U.S.-based KLA alone controls a majority of the process control tools market. VerWey, "U.S. Semiconductor Manufacturing Equipment," 5.

[165] A low manufacturing error rate corresponds to a high "yield."

[166] Robert Maire, "ASML EUV China Chip Equip Risk," *SemiWiki*, January 10, 2020, https://semiwiki.com/semiconductor-services/semiconductor-advisors/281384-asml-euv-china-chip-equip-risk/.

[167] Electrical instruments (e.g. C-V & DLTS plotters) measure electrical properties of wafers and films.

[168] Film and wafer measuring tools measure film thickness, makeup, and stack (e.g. fourier transform infrared spectrometers, ellipsometers, opto-acoustic tools, and x-ray tools), and wafer surfaces, taper, warpage, and bow (e.g. wafer flatness mapping tools, surface profiling tools, optical instruments, and atomic force microscopes).

[169] CD measuring tools (including optical tools and scanning electron microscopes) measure device dimensions and ensure alignment between a photomask and wafer during photolithography.

[170] Defect inspection tools detect and analyze wafer defects. Such tools include brightfield inspection tools (using light to scan the wafer), darkfield inspection tools (using lasers), e-beam inspection tools (using electrons), and optical and scanning electron microscopes.

[171] General purpose microscopy tools include scanning electron microscopes and transmission electron microscopes.

[172] A structural inspection tool uses a focused ion beam to inspect wafer structures.

[173] "TFX3000-Optical measuring equipment," RSIC, accessed November 27, 2020, http://en.rsicsh.com/ProductsStd_190.html.

[174] For example, RSIC's CD measuring tools can analyze FinFETs, which are transistors used for advanced nodes. "TFX3000 OCD -- 300mm fully automatic optical critical dimension and shape measurement system," RSIC, accessed November 27, 2020, http://en.rsicsh.com/ProductsStd_191.html.

[175] SEMI, "China IC Ecosystem," 36.

[176] "Products & Solutions > Semiconductor," Grand Tec, accessed September 4, 2020, http://www.grand-tec.com/en/Products_Solutions/Semiconductor.html; "Wafer Automatic Optical Inspection Equipment," SMEE, accessed September 4, 2020, http://www.smee.com.cn/eis.pub?service=homepageService&method=indexinfo&onclicknodeno=1_4_1_3.

[177] Assembly inspection tools inspect dies, bonding, packages, or wafers for defects throughout the packaging process.

[178] Dicing tools cut individual chips (dies) in the wafer into separated chips. This process also involves thinning the wafer. Dicing tools include blade saws, laser saws, dicing accessories and backside grinding.

[179] Bonding tools include die attach tools (to connect dies to lead frames or substrates), wire bonders (to make interconnects between lead frames and die pads), and advanced interconnect tools.

[180] Packaging tools encase dies in packages.

[181] Integrated assembly tools integrate different packaging systems.

[182] SoC test tools can test logic, memory, mixed, and analog circuits. As a result, they can test a wide variety of chips, including advanced logic chips like GPUs and other processors.

[183] Linear devices include, for example, operational amplifiers and voltage regulators.

[184] Burn-in tools heat devices to check if defects cause devices to fail.

[185] Handler and probers link test tools and tested devices.

[186] U.S.-based Teradyne says most of its testing equipment is manufactured in China. Teradyne, "Comment on Advanced Notice of Proposed Rulemaking Regarding Review of Controls for Certain Emerging Technologies," BIS-2018-0024-0057, https://www.regulations.gov/document?D=BIS-2018-0024-0057.

[187] Ding Yi, "China's Tztek to Acquire German Firm to Enter Semiconductor Testing Market," *Caixin Global*, June 23, 2020, https://www.caixinglobal.com/2020-06-23/chinas-tztek-to-acquire-german-firm-to-enter-semiconductor-testing-market-101571420.html.

[188] EDA market shares for the United States, Japan, the U.K., and Israel are from Rhines, "Electronic Design Evolution," 34. As Rhines excludes China, China's market share is estimated based on reported Chinese EDA tool revenue of $50 million in "Current Status of the Integrated Circuit Industry in China — EDA Industry Review," *J. Microelectron. Manuf.*, Vol. 2, No. 3 (September 29, 2019): 1, http://www.jommpublish.org/p/36/. The non-Chinese market shares are adjusted to account for inclusion of China's market share. Core IP market shares are based on Antonio Varas and Raj Varadarajan, "How Restricting Trade with China Could End US Semiconductor Leadership" (Boston Consulting Group, March 9, 2020), 9, https://www.bcg.com/publications/2020/restricting-trade-with-china-could-end-united-states-semiconductor-leadership.aspx; and Peter Clarke, "Synopsys above ARM in IP licensing revenue in 2019," *eeNews Analog*, March 25, 2020, https://www.eenewsanalog.com/news/synopsys-above-arm-ip-licensing-revenue-2019.

[189] The $6.8 billion figure includes four segments in the EDA market: computer-aided engineering (CAE) for chip logic design, i.e., the abstract layout and connectivity of transistors; design of printed circuit boards (PCB) and multi-chip modules (MCM); and chip

physical design and verification, i.e. the translation of logic design into a physical layout of transistors and interconnects within the chip; and services. "ESD Alliance Reports EDA Industry Revenue Increase for Q4 2019," *Electronic System Design Alliance*, March 25, 2020, http://esd-alliance.org/wp-content/uploads/PDFs/2020/MSS_Q4_2019_PressRelease_FINAL.pdf. Although sometimes included in the EDA market, this report separates the core IP market. Clarke, "Synopsys above ARM."

[190] Since 2017, Mentor graphics has been a U.S. subsidiary of the German firm Siemens. "Siemens closes Mentor Graphics acquisition," *Mentor*, March 30, 2017, https://www.mentor.com/company/news/siemens-closes-mentor-acquisition.

[191] ARM is owned by the Japan-based Softbank. However, an offer from Nvidia to acquire ARM is pending.

[192] Four U.S.-based firms control most of the EDA market: Synopsis (36.5 percent), Cadence (24.7 percent), Mentor Graphics (15.3 percent), and Ansys (12.9 percent). Cheng Ting-Fang and Laury Li, "The great US-China tech decoupling: Where are we now?," *Nikkei Asia*, December 30, 2019, https://asia.nikkei.com/Economy/Trade-war/The-great-US-China-tech-decoupling-Where-are-we-now.

[193] "Cadence Design Systems: Winner In An Oligopoly EDA Industry," *Seeking Alpha*, August 29, 2016, https://seekingalpha.com/article/4002863-cadence-design-systems-winner-oligopoly-eda-industry; Stewart Randall, "SILICON | China's design tools conundrum," *TechNode*, November 7, 2019, https://technode.com/2019/11/07/silicon-chinas-design-tools-conundrum/; Luffy Liu, "China and it's Pursuit for Chip Self-Sufficiency (Part 2)," *EETimes China*, April 16, 2019, https://www.eetasia.com/news/article/China-and-its-Pursuit-for-Chip-Self-Sufficiency-Part-2.

[194] Saar Drimer, "EDA is dead. What comes next is exciting," *Medium*, May 3, 2016, https://medium.com/@saardrimer/eda-is-dead-what-comes-next-is-exciting-cd5f3301402b. The field also includes several open-source tools. Notably, DARPA and Synopsys are partnering in the development of an open-source EDA tool for verification of analog and mixed-signal designs. "Synopsys Awarded DARPA ERI Contract Extension for Analog/Mixed-Signal Emulation Technology Innovation," *Synopsys*, July 15, 2019, https://news.synopsys.com/2019-07-15-Synopsys-Awarded-DARPA-ERI-Contract-Extension-for-Analog-Mixed-Signal-Emulation-Technology-Innovation.

[195] Stewart Randall, "SILICON | Why Chinese EDA tools lag behind," *TechNode*, November 13, 2019, https://technode.com/2019/11/13/silicon-why-chinese-eda-tools-lag-behind/; "EDA Industry Review," 3. Many Chinese EDA firms, including Xpeedic, were founded or are run by former employees of U.S. EDA firms. Rhines, "Electronic Design Evolution," 36.

[196] Empyrean is owned by China Electronics Corporation, the largest state-owned enterprise (SOE) in China, and a supporting unit for the National Engineering Research Center for Large Scale Integrated Circuit CAD and responsible for national R&D for EDA. In the last five years, Empyrean has experienced a CAGR of 50 percent and has recruited three international EDA experts via China's Thousand Talents plan. Empyrean started with $5.8 million in financing in 2009 and by September 2018, additional funding rounds including a $3.5 million investment from the National IC fund gave Empyrean $25 million of registered capital. This was the first time the National IC fund invested in an EDA software firm, and it may increase its Empyrean holdings in the future.

[197] "Empyrean's EDA Software," Ambition Technologies, accessed September 4, 2020, https://www.ambitec.org/products-1/vlsi-ams-ic-design/ams-design/; Randall, "Why Chinese EDA tools lag behind." Empyrean also provides system-on-chip (SoC) design optimization solutions. Over 85% of the major Chinese fabless firms use Empyrean's SoC design optimization and circuit simulation tools.

[198] Randall, "Why Chinese EDA tools lag behind."

[199] Randall, "China's design tools conundrum"; "EDA Industry Review," 3.

[200] "EDA Industry Review," 3. For more Chinese firms and their capabilities, see "EDA Industry Review," 2.

[201] Randall, "Why Chinese EDA tools lag behind"; "EDA Industry Review," 3. U.S. EDA firms also have a captive customer base because engineers were trained on their tools since university. Randall, "Why Chinese EDA tools lag behind."

[202] Cheng Ting-Fang and Laury Li, "China aims to shake US grip on chip design tools," *Nikkei Asia*, November 25, 2020, https://asia.nikkei.com/Business/China-tech/China-aims-to-shake-US-grip-on-chip-design-tools; Josh Horwitz, "Intel Capital invests in Chinese chip companies amid tech tensions," *Reuters*, May 13, 2020, https://www.reuters.com/article/us-intel-investments-china/intel-capital-invests-in-chinese-chip-companies-amid-tech-tensions-idUSKBN22P0GK.

[203] Rick Merritt, "DARPA Unveils $100M EDA Project," *EE Times*, June 27, 2018, https://www.eetimes.com/darpa-unveils-100m-eda-project/.

[204] Simon Sharwood, "Brit chip design company Imagination Tech sold to China-linked private equity," *The Register*, September 25, 2017, https://www.theregister.com/2017/09/25/imagination_technologies_sold_to_private_equity/.

[205] Cheng Ting-Fang and Laury Li, "Arm China asks Beijing to intervene in row with UK parent," *Nikkei Asia*, July 28, 2020, https://asia.nikkei.com/Business/China-tech/Arm-China-asks-Beijing-to-intervene-in-row-with-UK-parent. ARM China still needs to license designs from parent ARM. Cheng Ting-Fang, "Beijing's latest tech ally in US clampdown: Arm

China," *Nikkei Asia*, December 4, 2019, https://asia.nikkei.com/Economy/Trade-war/Beijing-s-latest-tech-ally-in-US-clampdown-Arm-China.

[206] Joel Hruska, "Cut Off From ARM, x86, What CPU Architectures Can Huawei Use?," *ExtremeTech*, May 23, 2019, https://www.extremetech.com/computing/291875-cut-off-from-arm-x86-what-cpu-architectures-can-huawei-actually-use; "A new blueprint for microprocessors challenges the industry's giants," *The Economist*, October 3, 2019, https://www.economist.com/science-and-technology/2019/10/03/a-new-blueprint-for-microprocessors-challenges-the-industrys-giants.

[207] Stewart Randall, "SILICON | Why China might block Nvidia-Arm deal," *TechNode*, September 18, 2020, https://technode.com/2020/09/18/silicon-why-china-might-block-nvidia-arm-deal/.

[208] Aditi Bhandari and Christian Inton, "China's Chip Challenge," *Reuters Graphics*, June 13, 2019, https://graphics.reuters.com/HUAWEI%20TECH-USA-CHIP-CATCHUP/010092PK3JW/index.html.

[209] United States Geological Survey, *Mineral Commodity Summaries 2020* (Reston VA: Department of the Interior, 2020), 7, https://pubs.usgs.gov/periodicals/mcs2020/mcs2020.pdf.

[210] Many key raw materials are abundant throughout Earth's crust, and processing materials requires less cost and complexity relative to other parts of the semiconductor supply chain. Therefore, many countries not currently producing certain raw materials can increase production in response to supply shocks. See the companion CSET report for more detail on China's ability to successfully apply export controls on raw materials discussed in this section. Khan, "Securing Semiconductor Supply Chains."

[211] "Semiconductor Materials growing to nearly $50B Market in 2020 after Downturn," *Techcet*, January 16, 2020, https://techcet.com/semiconductor-materials-growing-to-nearly-50b-market-in-2020-after-downturn/.

[212] Techcet, "Semiconductor Materials." For SEMI's estimates on historical wafer revenues, see "2019 Global Silicon Shipments Dip From 2018 Record High But Revenue Remained Stable Above $11 Billion, SEMI Reports," *SEMI*, February 4, 2020, https://www.semi.org/en/news-resources/press/2019-global-silicon-shipments.

[213] "Webinar: Turning the Tide for Semiconductor Manufacturing in the U.S.," Semiconductor Industry Association, September 18, 2020, https://www.semiconductors.org/events/webinar-turning-the-tide-strengthening-the-u-s-position-in-semiconductor-manufacturing.

[214] It excludes the noble gases neon, argon, krypton, and xenon. It also excludes more abundant gases such as oxygen and nitrogen.

[215] USGS, *Mineral Commodities Summaries 2020*. China is also increasing production of gallium arsenide and gallium nitride. Dieter Ernst, "China's Bold Strategy for Semiconductors--Zero-Sum Game or Catalyst for Cooperation?" (Honolulu, HI: East-West Center, September 2016), 11, https://www.eastwestcenter.org/publications/chinas-bold-strategy-semiconductors-zero-sum-game-or-catalyst-cooperation.

[216] Shannon Davis, "Rare Earth Elements Supply Uncertain for IC Fabs," *Semiconductor Digest*, July 29, 2020, https://www.semiconductor-digest.com/2020/07/29/rare-earth-elements-supply-uncertain-for-ic-fabs/.

[217] For data, including countries included in "Rest of World," see USGS, *Mineral Commodities Summaries 2020*. As the USGS has not published later figures for U.S. boron, bismuth, germanium, and zinc production, we respectively used 2005, 2013, 2011, and 2002 numbers. For tungsten and zinc, as actual production numbers were unavailable, we used production capacity numbers instead. For phosphorus, the numbers are based on phosphate rock; for carbon the numbers are based on graphite; for salt and chlorine, the numbers are based on sodium chloride; and for fluorine, the numbers are based on fluorspar. Finally, the figure excludes hafnium as USGS data is unavailable.

[218] USGS, *Mineral Commodities Summaries 2020*. The uncategorized number is a result of limitations in the dataset. This number includes production by several of the other listed countries and regions.

[219] Most Chinese materials firms focus on lower end processes, and do not support materials for processing 300 mm wafers. For an analysis of China's key materials firms' capabilities, see "Current Status of the Integrated Circuit Industry in China — Overview of Semiconductor Materials Industry" *J. Microelectron. Manuf.*, Vol. 3, No. 1 (March 30, 2020), http://www.jommpublish.com/p/51/.

[220] Shin-Etsu ($3.5 billion in revenue) has manufacturing sites in China, the Netherlands, Thailand, Taiwan, South Korea, and the United States. Siltronic ($1.6 billion) has manufacturing sites in Germany, Singapore, and the United States. SUMCO ($2.9 billion) has manufacturing sites in Japan. GlobalWafers ($1.9 billion) has manufacturing sites in Italy, Japan, Malaysia, South Korea, Taiwan, and the United States. SK Siltron has $1.1 billion in revenue. CSET analysis of firm financial statements.

[221] Okmetic is a Finnish firm that was acquired by a Chinese state investment fund. "China's National Silicon Pays $195M For Semiconductor Co.," *Law360*, April 1, 2016, https://www.law360.com/articles/779240. It has about $91 million in annual revenue.

[222] "Global $4.97 Billion Photomask Market (2019 to 2026) - Key Players Include Applied Materials, Photronics & LG Innotek Among Others - ResearchAndMarkets.com," *Business Wire*, March 18, 2020, https://www.businesswire.com/news/home/20200318005581/en/Global-4.97-Billion-Photomask-Market-2019-2026.

[223] "Photoresist & Photoresist Ancillaries Market," *Markets and Markets*, January 2020, https://www.marketsandmarkets.com/Market-Reports/photoresist-market-184731291.html; "Photoresist And Photoresist Ancillaries Market Size," *Global Market Insights*, 2016, https://www.gminsights.com/industry-analysis/photoresist-and-photoresist-ancillaries-market. A $1.6 billion subset of the market covers photoresists used in photolithography.

[224] "2020 Global CMP Polishing Pad Market Outlook," *360 Market Updates*, December 4, 2019, https://www.360marketupdates.com/2020-global-cmp-polishing-pad-market-14739277.

[225] Julissa Green, "Sputtering Target: An Important Component of Semiconductor Materials," *Stanford Advanced Materials*, July 3, 2018, https://www.sputtertargets.net/the-sputtering-target-an-important-component-of-semiconductor-materials.html.

[226] "Electronic Gases Market," *Markets and Markets*, accessed September 4, 2020, https://www.marketsandmarkets.com/Market-Reports/electronic-gases-market-17123047.html; Michael A. Fury, "It's a Materials World – With Positive Forecast," *SEMI*, June 30, 2015, http://www1.semi.org/en/node/56701.

[227] In 2018, the electronic gas market was $6 billion, of which specialty gases took $3.4 billion, with common gases taking much of the rest. Mike Corbett and Andy Tuan, "Opportunities in Electronic Specialty Gases," *SEMI*, October 9, 2019, https://blog.semi.org/technology-trends/opportunities-in-electronic-specialty-gases.

[228] Yuko Hampton, SUMCO Phoenix Corporation, "Comments on Section 301, Chapter 28, Carbides of silicon in grains," USTR-2018-0026, https://beta.regulations.gov/comment/USTR-2018-0026-0899.

[229] For a diagram of the process of wafer production, see Eric D. Williams, Robert U. Ayres, and Miriam Heller, "The 1.7 Kilogram Microchip: Energy and Material Use in the Production of Semiconductor Devices," *Environ. Sci. Technol.*, Vol. 36, No. 24, 5504–5510 (October 5, 2002), https://pubs.acs.org/doi/10.1021/es025643o.

[230] Silicon, which is abundant in Earth's crust, is by far the most commonly used material—and virtually exclusively used for leading-edge commercial chips.

[231] Gallium-based materials (gallium arsenide and gallium nitride), germanium, silicon carbide, and a number of indium-based materials. "Semiconductor Materials Where do Semiconductor Raw Materials Come From?," The Chip Source, accessed September 4, 2020, http://thechipsource.com/semiconductor-materials-where-materials-come-from.html. Gallium arsenide, gallium nitride, germanium, and silicon carbide are used for certain high-speed or high-temperature chips. Kathy Pretz, "IEEE Plots a Path for Wide Bandgap Semiconductors Used in the Power Industry," *IEEE Spectrum*, March 24, 2020, https://spectrum.ieee.org/the-institute/ieee-news/ieee-plots-a-path-for-wide-bandgap-semiconductors-used-in-the-power-industry. Gallium-based chips' ability to withstand high

temperatures make them suitable for defense applications, although silicon can substitute for commercial applications. John Adams, "Remaking American Security" (Washington, DC: Alliance for American Manufacturing, May 2013), 60, https://docs.house.gov/meetings/FA/FA14/20130725/101216/HHRG-113-FA14-Wstate-AdamsB-20130725.pdf. Indium-based materials are used for laser diodes and LEDs.

[232] Most wafers are often made primarily of a single material, such as silicon. However, more complex wafers include epitaxial (EPI) wafers and silicon-on-insulator (SOI) wafers. In an EPI wafer, a non-silicon material is added on top of a silicon wafer as a layer in which transistors and other devices are later made. In an SOI wafer, the top-most layer of silicon is placed on an insulator layer within the wafer.

[233] Silicon dopants include boron, aluminum, phosphorus, arsenic, antimony, bismuth, lithium, nitrogen, gold, platinum, gallium, indium, and germanium. The noble gas xenon is used in ion beams to process silicon. Dopants for other wafer materials include some of the above but additionally tellurium, sulphur, tin, beryllium, zinc, magnesium, carbon, chlorine, sodium, fluorine, germanium, silicon, indium, and gallium.

[234] SEMI, "World Fab Forecast," November 2020 edition.

[235] Mark LaPedus, "Mixed Outlook For Silicon Wafer Biz," *Semiconductor Engineering*, February 21, 2019, https://semiengineering.com/mixed-outlook-for-silicon-wafer-biz/.

[236] SEMI, *China IC Ecosystem*, 31. These Chinese-made wafers include silicon wafers, EPI wafers, or SOI wafers.

[237] "World Fab Forecast" (Milpitas, CA: SEMI, November 2020 edition); SEMI, "China IC Ecosystem," 31. For China's wafer production capacity, we exclude Chinese-owned, Finland-based Okmetic but include the other eight Chinese firms.

[238] Throughout, the term "photomask" is intended to additionally include reticles. A photomask's pattern has a 1:1 correspondence to a desired wafer pattern, while a reticle's pattern corresponds to only part of a desired wafer pattern. Therefore, the reticle must be moved relative to the wafer to transfer the reticle's pattern multiple times to create a repeating pattern on the wafer.

[239] DUV photomasks are made of chrome on a glass substrate, while EUV masks use silicon and molybdenum. Mark LaPedus, "Mask Maker Worries Grow," *Semiconductor Engineering*, August 18, 2016, https://semiengineering.com/what-mask-makers-want/.

[240] For photomask firm M&A history, see Photronics, "Form 8-K," May 23, 2018, 17, https://photronicsinc.gcs-web.com/static-files/27d9a55b-79bb-4bc6-a6cf-95b471fa9e05.

[241] David Manners, "Photomask market surges 13%, says SEMI," *Electronics Weekly*, April 10, 2018, https://www.electronicsweekly.com/news/business/525001-2018-04/.

[242] "The Mask Maker Survey 2016," *eBeam Initiative*, 2016, https://www.ebeam.org/docs/ebeam_survey_mask_2016.pdf.

[243] "Mask Operation," SMIC, accessed September 4, 2020, https://www.smics.com/en/site/mask.

[244] "Factbox: The high-tech materials at the heart of a Japan-South Korea row," *Reuters*, July 2, 2019, https://www.reuters.com/article/us-southkorea-japan-laborers-factbox/factbox-the-high-tech-materials-at-the-heart-of-a-japan-south-korea-row-idUSKCN1TX12I.

[245] Samuel M. Goodman, Dan Kim and John VerWey, *The South Korea-Japan Trade Dispute in Context: Semiconductor Manufacturing, Chemicals, and Concentrated Supply Chains* (Washington, DC: U.S. International Trade Commission, October 2019), 17–19, https://usitc.gov/publications/332/working_papers/the_south_korea-japan_trade_dispute_in_context_semiconductor_manufacturing_chemicals_and_concentrated_supply_chains.pdf.

[246] Several ancillary materials are used along with photoresists. A material called a developer is used to dissolve the light-exposed parts of the photoresist. Anti-reflective coatings are applied to a wafer before or after depositing a photoresist to stabilize the photolithography process. Photoresist removal chemicals remove remaining photoresist after photoresist processing and/or etching.

[247] Individual segments are: EUV (market size of $10 million), ArF immersion ($720 million), ArF ($300 million), KrF ($330 million), and g-line/i-line ($250 million). Shannon Davis, "EUV Materials Small But Strategic Fraction of $1.6B IC Photoresists Market," *Semiconductor Digest*, March 11, 2020, https://www.semiconductor-digest.com/2020/03/11/euv-materials-small-but-strategic-fraction-of-1-6b-ic-photoresists-market/.

[248] SEMI, "China IC Ecosystem," 32.

[249] "Photoresist Market 2019 Global Key Players, Demands, Revenue, Share, Competitive Landscape and Forecasts to 2025," *PR Newswire*, August 7, 2019, https://www.prnewswire.com/in/news-releases/photoresist-market-2019-global-key-players-demands-revenue-share-competitive-landscape-and-forecasts-to-2025-877499817.html.

[250] "Global and China Photoresist Industry Report, 2019-2025 Featuring 14 Global and 10 Chinese Photoresist Vendors," *Business Insider*, August 7, 2019, https://markets.businessinsider.com/news/stocks/global-and-china-photoresist-industry-

report-2019-2025-featuring-14-global-and-10-chinese-photoresist-vendors-1028425947.

[251] Michael D. Wedlake, "Challenges & Opportunities in Post CMP Cleans Innovation," Surface Preparation and Cleaning Conference 2018, Boston, MA, April 9, 2018, 3, https://linxconferences.com/wp-content/uploads/2018/04/Michael-Wedlake-Business-of-Cleans.pdf.

[252] Slurries often include rare earth materials. Mark LaPedus, "Searching For Rare Earths Again," *Semiconductor Engineering*, February 19, 2015, https://semiengineering.com/searching-for-rare-earths-again/. Slurries are often used to planarize aluminum, copper for use in interconnects, tungsten, silicon, various oxides including silicon oxides used for insulative layers, and materials for "vias" which are electrical interconnects that pass through silicon layers. "Positive Forecasts for Electronic Gases, CMP Consumables, and Sputtering Targets," *SEMI*, December 4, 2012, http://stg7.semi.org/en/node/44151.

[253] "Global CMP Slurry Market 2019 By Manufacturers, Regions, Type and Application, Forecast to 2024," *Market Reports World*, February 1, 2019, https://www.marketreportsworld.com/global-cmp-slurry-market-13046952.

[254] SEMI, "China IC Ecosystem," 21.

[255] For example, Anji makes slurries for use in depositing silicon oxides, copper, and vias. SEMI, "China IC Ecosystem," 32.

[256] Fury, "Materials World"; SEMI, "China IC Ecosystem," 32.

[257] Fury, "Materials World." Some of these materials are used to form interconnects, which are wires that connect devices, such as transistors, within a chip. Interconnects for silicon-based chips were historically made of aluminum but now are typically made of copper, and increasingly, cobalt. Tungsten or silicon-based materials are used for shorter interconnects. Titanium nitride is also used as a barrier metal surrounding copper interconnects. Anderson Pires Singulani, "4.1 Properties of Interconnect Materials," Advanced Methods for Mechanical Analysis and Simulation of Through Silicon Vias, Dissertation, Vienna University of Technology, June 2014, https://www.iue.tuwien.ac.at/phd/singulani/dissse12.html. Other materials can be used for deposition of insulators that form layers within transistors and also between interconnects. Insulators include silicon oxide, aluminum oxide, titanium dioxide, tantalum pentoxide, hafnium dioxide, hafnium silicate, lanthanum oxide, zirconium oxide, and zirconium silicate. Mark T. Bohr, Robert S. Chau, Tahir Ghani and Kaizad Mistry, "The High-k Solution," *IEEE Spectrum*, October 1, 2007, https://spectrum.ieee.org/semiconductors/design/the-highk-solution. Lanthanum oxide is derived from the rare earth element lanthanum. LaPedus, "Searching For Rare Earths."

[258] Fury, "Materials World." Materials include tungsten, titanium, aluminum, tantalum, copper, precious metals, nickel, cobalt, and multicomponent alloys. Alloys include nick-

chrome alloy, nickel-cobalt alloy. Targets can also include ceramic compounds such as oxides, silicides, carbides, and sulfides. Green, "Sputtering Target." Market sizes are: precious metals ($380 million), tungsten ($20 million), titanium ($180 million), aluminum ($80 million), tantalum ($240 million), and copper ($110 million). Shannon Davis, "Cobalt and Nickel Targets Super Strategic for IC Fabs," *Semiconductor Digest*, November 25, 2019, https://www.semiconductor-digest.com/2019/11/25/cobalt-and-nickel-targets-super-strategic-for-ic-fabs/.

[259] KFMI produces sputtering targets and ancillaries, while Grikin produces sputtering targets for ultra-pure aluminum alloy. SEMI, "China IC Ecosystem," 32.

[260] Speciality electronic gases like nitrogen trifluoride, tungsten hexafluoride, hydrogen chloride, ammonia, disilane, germane, high-purity carbon dioxide, nitrous oxide. Other electronic gases also include common gases like nitrogen, hydrogen, helium, argon helium, and carbon dioxide. "Leading in electronic gases," *Linde Electronics*, 2016, 7–8, https://www.linde-gas.com/en/images/Linde%20Electronics%20brochure_tcm17-279892.pdf. Photolithography involves the use of various noble gases (e.g. neon, argon, and krypton) to create lasers to draw circuit patterns on wafers. Ukraine is a major supplier of highly purified neon. Geopolitical instability in Ukraine in 2014 resulted in supply shocks of highly purified neon. Goodman et al., *The South Korea-Japan Trade Dispute*, 3; Fury, "Materials World." However, noble gases including neon can be obtained from the atmosphere from any part of the world—so no country can guarantee exclusive production of highly purified versions of these gases over the long-term. The most advanced photolithography equipment, EUV, uses a tin light source rather than a gas-based light source.

[261] Fury, "Materials World."

[262] SEMI, "China IC Ecosystem," 32.

[263] Mordor Intelligence, "Web Chemicals Market."

[264] Key wet chemicals include sulfuric acid, isopropyl alcohol, ammonium hydroxide, phosphoric acid, nitric acid, hydrochloric acid, acetic acid, among others. "Wet Chemicals Market For Electronics & Semiconductor Applications - Growth, Trends, and Forecast (2020 - 2025)," *Mordor Intelligence*, 2019, https://www.mordorintelligence.com/industry-reports/wet-chemicals-market-for-electronics-and-semiconductor-applications. For more information on chemicals used in the semiconductor industry, see Sunju Kim et al., "Chemical use in the semiconductor manufacturing industry," *Int J Occup Environ Health*, Vol. 24, No. 3–4 (October 3, 2018): 109–118, https://www.ncbi.nlm.nih.gov/pmc/articles/PMC6237170/.

[265] SEMI, "China IC Ecosystem," 32.

[266] Bond wires are typically made of aluminum, copper, silver, or gold.

[267] The lead frame manufacturing process can also require the use of copper or a combination of iron and nickel. "The economic manufacture of lead frames – a technical comparison," Precision Micro, accessed September 4, 2020, https://www.precisionmicro.com/the-economic-manufacture-of-lead-frames-a-technical-comparison/.

[268] "IC Packaging," *Millennium Circuits Limited*, December 4, 2017, https://www.mclpcb.com/ic-packaging-information/.

[269] "Die Attach Adhesives and Materials," *EESemi*, 2005, https://www.eesemi.com/DA_matls.htm.

[270] SEMI, "China IC Ecosystem," 32; Dan Tracy, Mark Thirsk, and Marcel Wieland, "Connected World: New Material Challenges and Solutions – Market Update and Outlook," *SEMI*, September 27, 2017, 22; Lara Chamness, "Materials Market To Top $50 Billion In 2013," September 20, 2012, https://semiengineering.com/materials-market-top-50-billion-2013/; "Ceramic IC Packages Market," *Transparency Market Research*, November 2020, https://www.transparencymarketresearch.com/ceramic-ic-packages-market.html.

[271] Khan, "Securing Semiconductor Supply Chains."

[272] Hunt et al., "China's Progress in Semiconductor Manufacturing Equipment."

[273] IC Insights, "McLean Report"; IC Insights, "O-S-D Report." This value differs from the WSTS estimate from Figure 5, which values the semiconductor market at $412.3 billion. We use IC Insights values for the purposes of this analysis to ensure consistency with later usage of IC Insights' estimates of fabless and IDM market sizes.

[274] OSAT market size is based on revenues of top 25 OSAT vendors. Yole Développement, "Advanced packaging."

[275] LaPedus, "OSAT Biz."

[276] "Pure-Play Foundry Market On Pace For Strongest Growth Since 2014," *IC Insights*, September 22, 2020, https://www.icinsights.com/news/bulletins/PurePlay-Foundry-Market-On-Pace-For-Strongest-Growth-Since-2014.

[277] Rhines, "Electronic Design Evolution," 24.

[278] Market sizes for fab equipment and ATP equipment each include a proportionate share of SME services market share.