What are FPGAs anyway and why is it fun to play with them?

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Who ? me !

Rudi van Drunen

- By day
  - CTO (SpronQ.com) and Devops
- By night
  - Hardware Geek (xlexit.com)
- Spare time
  - Landscape photography

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Overview

- What is an FPGA
- What is it used for
- Getting started
  - Hardware
  - Software
- Why is it fun ? : Demo

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Hardware

Evolution

- Tubes - Transistors
- Integrated circuits
- “Standard” logic (ie. TTL circuits)
- Complex programmable logic
- ASIC
- Full custom

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FPGA

Programmable hardware

- PAL
  - Just combinatory logic
  - Often One time flash
- FPGA Field Programmable Gate Array
  - Semi Custom
  - Combinatory logic and FlipFlops
  - (dynamic) configuration on power up
  - Function Blocks (even complete processor cores)
- ASIC Application Specific Integrated Circuit
  - Full custom
  - Complex development cycle
  - You need a foundry, and $$

Applications

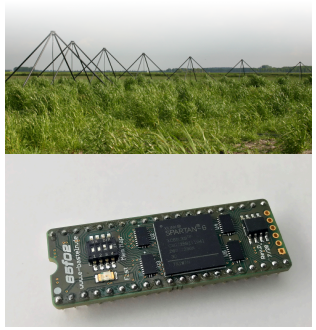
Programmable logic

- Anywhere you need gates and logic elements
  - Glue between processor / IO / memory
  - Complex algorithms (co-processor)
  - Bus interfacing (PCI bus)
  - Flexibility
    - no new PCB
    - on the fly reconfigurable (Hardware becomes Software)

FPGAs

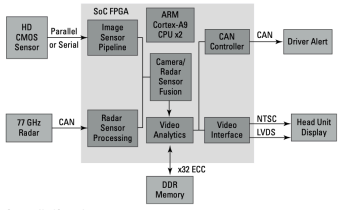
Applications

- LOFAR
  - signal processing
- Bitcoin mining
- Rebuilding (retro) processors
  - `http://www.e-basteln.de/computing/65f02/65f02/`
- High performance (custom) computing
- Data Processing (5G, Image, Medical, AI)



Example

Automotive vision system



Courtesy of Intel Corporation.

FPGA

Advantages / Disadvantages

- Latency (+)
  - low latency (< 1μs opposite of > 10μs for processors)
- Connectivity / Bandwidth (+)
  - direct connect to io (sensors)
- Engineering cost (-)
  - longer leadtimes (LONG compile (routing optimizations) times, complex languages)
    - Verilog, VHDL
    - High level synthesis (OpenCL, C++)
- Energy Efficiency (+)

Power / Efficiency

- Monte Carlo simulation

Platform	Power (W)	Bsim/s	Msim/s/W
CPU	130	0,032	0,0025
GPU	210	10,1	48
FPGA	45	12,0	266

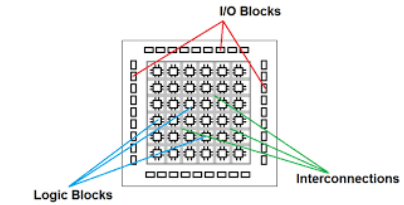
FPGA vendors

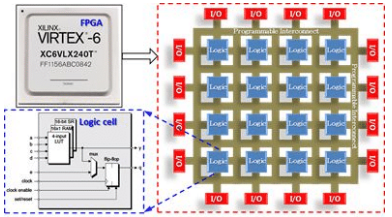
- Xilinx
  - 5G beam forming FPGAs
- Intel
  - SoC with integrated FPGA
- Lattice
  - GP FPGAs
- QuickLogic
- Achronix
  - integrated 400G ethernet

FPGA

Field Programmable Gate Array

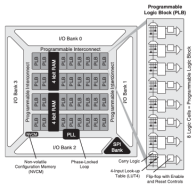
- Array of logic elements (blocks)
  - LUT
  - FF
- I/O elements
- Programmable interconnect array
- Glue logic (load configuration)

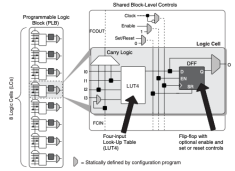


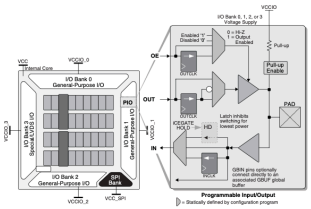


FPGA internals

Blocks





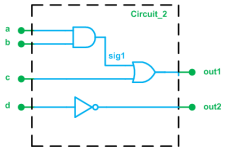


Workflow

- Design functionality
- Design blocks
- program blocks
  - VHDL
  - Verilog
- Compile, synthesis, place and route
- simulate (timing)
- verify, and generate bitstream
- Flash bitstream to FPGA

VERILOG

Hardware design language




```
1   module Circuit_2
2       (
3       input wire a,
4       input wire b,
5       input wire c,
6       input wire d,
7       output wire out1,
8       output wire out2
9       );

10      wire sig1;
11      assign sig1 = a & b;
12      assign out1 = sig1 | c;
13      assign out2 = ~ d;

14  endmodule
```


DIY

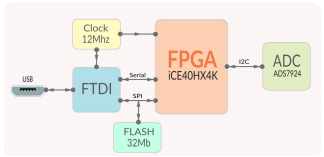
Hardware

- `http://fpgawars.github.io`
- Lattice iCE40HX4K
  - 3520 cells, 95 pins, 250MHz
  - I2C SPI cores LVDS bridge 24mA drive
  - `https://www.latticesemi.com/en/Products/FPGAandCPLD/iCE40`
- Alhambra
  - `https://github.com/FPGAwars/Alhambra-II-FPGA`
  - Arduino compatible

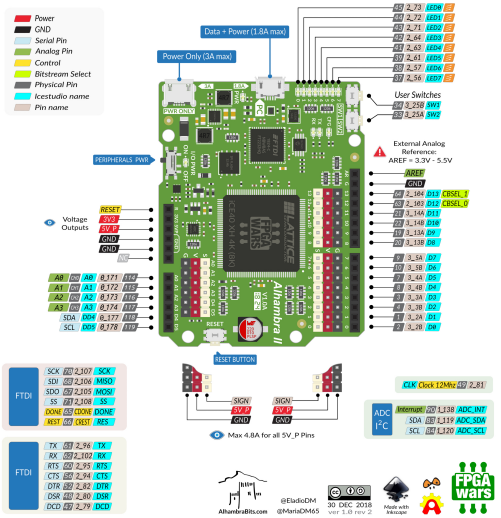
Alhambra II board

Connections

- https://github.com/FPGAwars/Alhambra-II-FPGA



- Maximum Supply Voltage: 5.5V
- Operating Supply Voltage: 3.5 - 5.5V
- 3.3V GPIO, 5V Compatible
- Each GPIO Includes a 200 ohm Serial Resistor
- ADC Internal to External Ref. Automatic Switching



DIY

software

- Dev environment
  - Vendor supplied software
    - ICEcube 2 (Lattice)
      - Windows, Linux
  - Open Source
    - icestudio IDE
    - Command-line tools

Questions so far !?

Demo Time !!

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Alhambra example

Self Balancing Robot

- https://www.mdpi.com/2079-9292/8/2/198/htm