CHARGE COUPLED AND CHARGE INJECTION DEVICE PERFORMANCE TRADEOFFS

R. D. Baertsch*

I. Introduction

This paper will review some of the performance tradeoffs between charge injection device (CID) and charge coupled device (CCD) imagers. The emphasis will be on a comparison between the CCD and CID approaches and no attempt will be made to differentiate in detail between the CCD frame transfer or interline transfer architectures and the CCD surface and bulk channel technology. These questions have been discussed extensively in recent books (1,2) and review articles (3,4) and some familiarity with these architectures and technologies will be assumed. The CID and the CCD frame transfer and interline transfer architectures are illustrated schematically in Fig. 1.

II. CID and CCD Readout Methods

The charge injection device (CID) will be differentiated from the charge coupled device (CCD) by the method of charge readout. In contrast to CCD's in which the signal charge is transferred sequentially to a readout amplifier at the edge of the array, as shown in Fig. 1, the CID confines this charge to an image site during sensing. The CID readout is obtained by sensing the displacement charge in an overlying electrode as the signal charge is transferred beneath two electrodes at the imaging site. In early CID structures (5), readout was obtained by injecting the charge associated with each site sequentially and measuring the substrate current. This sequential charge injection is not essential to the CID approach and parallel injection of the charge from an entire row or column of imaging sites has been described more recently (6). Charge injection itself is not an essential feature of the CID approach since after readout of a row of imaging sites the charge can be transferred in parallel to a diffused collector.

The readout of the CID is achieved by sensing the change in voltage on, say, a row electrode as charge is transferred at a single imaging site. The signal charge is delivered to the capacitance of an electrode overlying many imaging sites, and in some designs the CID is limited by reset noise in

*General Electric Corporate Research and Development, New York.

precharging the electrode capacitance or amplifier noise. For low capacitance designs, however, the performance of a CID imager is limited by dark current at room temperature.

CCD readout is effected by delivering the signal charge to an output node, either a diffused node (7) or a floating gate (8). At room temperature the dynamic range of CCD arrays is often limited by dark current, or more specifically by pattern noise on the dark current rather than amplifier noise or reset noise.

III. Features of the CID Approach

One feature of the CID approach stems directly from the chip architecture which does not require high charge transfer efficiency. Since the charge transfers back and forth at each imaging site, charge left behind on one transfer is recollected on the next. In contrast, CCD imagers require high transfer efficiency for readout of the signal charge without image smearing. For example, a 188 x 244 two-phase interline transfer CCD array requires a minimum of 864 transfers for the imaging site farthest from the readout amplifier. For a 20% transfer deficit in the worst case, a transfer inefficiency of 2.3×10^{-4} per transfer is necessary. For the three phase frame transfer arrays, even higher transfer efficiency will be required. This level of charge transfer inefficiency can only be obtained with the buried channel technology (9) or with surface channel devices operated with a background charge. In the latter case, non-uniformities in the electrical insertion of background charge will be an appreciable noise source, especially in the frame transfer architecture.

The excellent antiblooming properties of the CID also follow directly from the chip architecture where each imaging site is surrounded by a field stop diffusion or a region of thick oxide. In either case, the surface is accumulated and overflow of charge along the surface is prevented. Since the CID is usually fabricated on epitaxial material, charge diffusion away from a well which is overfilled is greatly attenuated. This architecture provides antiblooming capability in both row and column directions. The antiblooming capability of a 188 x 244 CID array is illustrated in Fig. 2 where a 1000X signal overload is shown.

The signal charge in the CID may be read out non-destructively, since the readout is obtained by transferring charge from under one electrode to the next at each imaging site. If the CID is cooled to -70°K, then dark current generation is negligible for integration times as long as 3 hours (10). Low light level imaging with a cooled CID can be accomplished by integrating a low light level scene for the desired time and reading out the same scene many times

to overcome the amplifier noise. If the CID is read out N times and the analog video data converted to digital and summed in a digital memory, the temporal noise sources are reduced by $\sqrt{N}$. Using this procedure, it is possible to achieve a noise level of 55 electrons with a CID array (11). A comparison of an image obtained with a single frame readout and a readout of 1600 summed frames has been published (11) Use of this non-destructive readout procedure to enhance the optical image of a planetary nebula is shown in Fig. 3 (11). Fig. 3 was obtained with a 1/2 hour exposure of a CID imager on the 4 meter Mayall telescope at Kitt Peak National Observatory.

The x-y addressing capability of the CID provides the possibility of non-sequential scan readout. For example, if a decoder similar to those used on an MOS random access memory were provided, then a completely random readout could be obtained. Applications for non-sequential scan readout include bandwidth compression of the video using transform techniques (12).

The CID approach presents a number of design and process-related features. Either high or low density arrays can be designed with the CID approach. Low density arrays have the advantage that the signal charge is collected from a large area while the dark current charge is generated only in the depletion region at the imaging site. Furthermore, CID imagers can be fabricated with either a standard p-channel non-overlapping gate MOS process or a more conventional CCD overlapping gate process.

The CID architecture, since it can be made without diffusions and only moderate transfer efficiency provides an excellent architecture for imagers on materials in which surface charge technology is not as advanced as silicon. CID imagers have been fabricated from both germanium (13) and InSb (14). The CID approach is particularly useful in the infrared where the useful image signal is often a small fraction of the background signal. Various readout schemes have been developed to subtract the background charge from the signal charge (14).

Finally, the CID architecture provides nearly complete utilization of the device area for active imaging sites. Up to 90% of the chip area can be used for active imaging sites in the CID, in contrast to the frame transfer and the interline transfer CCD's where less than half the chip area is used for imaging. Moreover, if these imaging sites are covered with a transparent electrode (15), nearly the theoretical silicon quantum efficiency can be achieved on a front

precharging the electrode capacitance or amplifier noise. For low capacitance designs, however, the performance of a CID imager is limited by dark current at room temperature.

CCD readout is effected by delivering the signal charge to an output node, either a diffused node (7) or a floating gate (8). At room temperature the dynamic range of CCD arrays is often limited by dark current, or more specifically by pattern noise on the dark current rather than amplifier noise or reset noise.

III. Features of the CID Approach

One feature of the CID approach stems directly from the chip architecture which does not require high charge transfer efficiency. Since the charge transfers back and forth at each imaging site, charge left behind on one transfer is recollected on the next. In contrast, CCD imagers require high transfer efficiency for readout of the signal charge without image smearing. For example, a 188 x 244 two-phase interline transfer CCD array requires a minimum of 864 transfers for the imaging site farthest from the readout amplifier. For a 20% transfer deficit in the worst case, a transfer inefficiency of 2.3×10^{-4} per transfer is necessary. For the three phase frame transfer arrays, even higher transfer efficiency will be required. This level of charge transfer inefficiency can only be obtained with the buried channel technology (9) or with surface channel devices operated with a background charge. In the latter case, non-uniformities in the electrical insertion of background charge will be an appreciable noise source, especially in the frame transfer architecture.

The excellent antiblooming properties of the CID also follow directly from the chip architecture where each imaging site is surrounded by a field stop diffusion or a region of thick oxide. In either case, the surface is accumulated and overflow of charge along the surface is prevented. Since the CID is usually fabricated on epitaxial material, charge diffusion away from a well which is overfilled is greatly attenuated. This architecture provides antiblooming capability in both row and column directions. The antiblooming capability of a 188 x 244 CID array is illustrated in Fig. 2 where a 1000X signal overload is shown.

The signal charge in the CID may be read out non-destructively, since the readout is obtained by transferring charge from under one electrode to the next at each imaging site. If the CID is cooled to -70°K, then dark current generation is negligible for integration times as long as 3 hours (10). Low light level imaging with a cooled CID can be accomplished by integrating a low light level scene for the desired time and reading out the same scene many times

side illuminated imaging device.

IV. Features of the CCD Approach

An important feature of CCD's for solid state imaging is that the signal charge is delivered to a low capacitance node, typically of order 1/4 pf. The signal voltage at this low capacitance node is large and a good signal-to-noise ratio is obtained. The noise associated with this type of output is of the order 200 electrons (1) and is primarily due to the reset noise associated with charging the node capacitance and the 1/f and thermal noise of the output amplifier. The noise can be greatly reduced using correlated double sampling (16) and values of 20 electrons have been obtained (17).

Even without correlated double sampling, it is possible to achieve sufficient signal-to-noise ratio that the performance of CCD imagers at room temperature is limited by dark current and not noise in the output amplifier. The dark current is reduced with cooling and the low light level performance of CCD imagers is improved.

High density arrays occur naturally with the CCD approach since adjacent electrodes must overlap to transfer charge. For a given silicon area, the best overall transfer efficiency is obtained by using the shortest possible electrodes. The close spacing between image sensing sites obtained by using short electrodes leads to high density arrays and high resolution at the focal plane of the imager.

Finally, CCD imagers can be used in a time delay and integrate mode because of the serial nature of the charge transfer. Here the imager is mechanically swept at a rate such that the charge associated with a given image point moves across the CCD at the same rate as the integrated charge is clocked along the array. This mode of operation can be used to improve the signal-to-noise ratio by the $\sqrt{N}$, where N is the number of times the charge is integrated as it transfers down the array. This technique is useful in a number of special applications, but it is especially useful in infrared imaging where the primary noise source is the shot noise associated with background radiation. This technique will improve the signal-to-noise ratio of a background noise limited imaging device by the $\sqrt{N}$.

VI. Performance Tradeoffs Between CID and CCD Imagers

In characterizing various solid state imagers, it is common to compare their limiting performance by quoting the minimum detectable signal in electrons. This number is usually derived by measuring the temporal noise at the output amplifier of the device and relating it to a mean

square noise charge. While this procedure may be useful in estimating the performance limit of a technology, it is not particularly helpful in evaluating practical imagers. There are a number of additional factors which are useful in the evaluation of imaging devices relative to a particular application. These factors will be discussed briefly before considering performance tradeoffs.

First, since the real input signal is optical, stating the noise in electrons is meaningful only if the quantum efficiency is stated. For example, an imager with 25% quantum efficiency will require a noise level 3 times lower than one with 75% quantum efficiency for the same noise equivalent photon signal.

Second, since the performance of an imager depends on signal-to-noise ratio, the signal handling capability of the imager is important. For example, surface channel devices may have an advantage over buried channel devices since their signal handling capability is larger.

Thirdly, since all room temperature silicon imaging devices are ultimately limited by shot noise on the dark current, the performance limit of the output amplifier is relatively unimportant as long as it is below the dark current level. In practice, it is not even the shot noise on the dark current which is the limitation, but the pattern "noise" associated with non-uniform generation of dark current from site to site. Thus, for many practical applications, the "noise" limit is not the temporal noise limit that is so widely quoted but rather pattern noise on the dark current or other kinds of pattern noise.

Because the CCD delivers its signal charge to a low capacitance node the reset noise and amplifier noise can be quite small and it is possible to obtain a signal-to-noise ratio which is limited by shot noise or pattern noise on the dark current at room temperature.

By using correlated double sampling to eliminate reset and amplifier noise low capacitance CID array designs can reach the same noise limit. A comparison of signal-to-noise ratio in the two devices then depends on the relative values of signal charge for the same photon input. Here the CID has an advantage over the interline transfer architecture which has opaque metal runs which obscure 1/2 of the input light (4). The CID has the additional advantage that the light is collected over a larger area than the area of the depletion region which is the source of most dark current. Thus at room temperature for low capacitance array designs the CID may have a slight advantage over the CCD while for arrays with larger electrode capacitance where amplifier noise

limits the CID the CCD may have a signal-to-noise advantage at room temperature.

For low temperature operation where dark current noise no longer limits performance the CCD has an advantage at low light levels for applications where rapid readout is desired. If repeated readout is acceptable the CID can achieve performance equivalent to CCD imagers.

Another area of comparison is anti-blooming. Here the CID array fabricated on epitaxial material has an advantage over both the CCD frame and interline transfer architectures.

Where non-sequential scan is required, such as in bandwidth reduction or various tracking applications the CID with random access addressing provides a unique capability.

CID imagers can be made with a simple single level metal process which leads to ease of manufacture. For those applications which require low cost and hence high yield, the process simplicity of the CID will be an advantage.

VII. Conclusions

The dynamic range of all silicon imagers is ultimately limited by shot noise or pattern noise on the dark current at room temperature. Since the reset and amplifier noise is small in the CCD approach, improved low light level performance is obtained by cooling below room temperature. CCD's can also be operated in a time delay and integrate mode.

CID imagers offer excellent anti-blooming performance and also provide some unique design and process flexibility. They can provide both a non-destructive and a random access readout capability.

Acknowledgments

I would like to acknowledge valuable discussions with C. H. Sequin, G. J. Michon and H. K. Burke. Thanks to G. W. Ludwig for a critical reading of this manuscript and J. O. Quesnel for outstanding cooperation in the preparation of this manuscript.

References

1. Sequin, C. H.; and Tompsett, M. F., "Charge Transfer Devices", Suppl. No. 8 to "Advances in Electronics and Electron Physics," Academic Press, Inc., New York 91975).

2. Jespers, P. J.; Van de Wiele, F. and White, M. H., "Solid State Imaging" Proceedings of the NATO Advanced Study Institute on Solid State Imaging, Lourvaine de Neuve, Belgium, Sept 1975.

3. Barbe, D. F., "Imaging Devices Using the Charge Coupled Concept", Proc. IEEE Vol. 63 pp 38-67 Jan (1975).

4. Barbe, D. F., "Charge Coupled and Charge Injection Device Imaging", IEEE Trans. on Elect. Dev. ED-23 pp 177-182 Feb (1976).

5. Michon, G. J.; Burke, H. K., "Charge Injection Imaging" Digest of Technical Papers, Int. Solid State Circuits Conf., Philadelphia, pp 138-139 (1973).

6. Michon, G. J.; Burke, H. K.; Brown, D. M., "Recent Developments in CID Imaging" Proc. of Symp. on Charge Coupled Devices for Technology for Scientific Imaging Applications, pp 106-115

7. Sequin, C. H.; Morris, F. J.; Shankoff, T. A.; Tompsett, M. F.; Zimany, E. J., "Charge-Coupled Area Image Sensor Using Three Levels of Polysilicon", IEEE Trans. on Elect. Dev. ED-21, pp 712-720, Nov (1974).

8. Wen, D. D., "Design and Operation of a Floating Gate Amplifier", IEEE J. of Solid State Circuits SC-9 pp 410-414, Dec (1974).

9. Jack, M. J.; Dyck, R. H., "Charge Transfer Efficiency in a Buried Channel CCD at Low Light Levels" IEEE Trans. of Electron Dev. ED-23 pp 228-234 Feb (1976).

10. Burke, H. K.; Michon, G. J., "Charge Injection Imaging: Operating Techniques and Performance Characteristics", IEEE Trans. on Elect. Dev. ED-23 pp 189-195 Feb (1976).

11. Aikens, R. S.; Lynds, C. R.; and Nelson, R. E., "Charge Injection Devices for Low Light Level Applications" Electro-optical Systems Design Conf., Anahiem, CA Nov 11-13 (1975).

12. Whitehouse, H. J., unpublished.

13. Wang, K. L.; Gray, P. V, unpublished.

14. Kim, J. C. "InSb MIS Technology and CID Devices", Proc. of 1975 Int. Conf. on the Application of Charge Coupled Devices, San Diego, CA pp 1-18.

15. Brown, D. M.; Ghezzo, M.; Garfinkel, M., "Transparent Metal Oxide Electrode CID Imager" IEEE Trans. on Elect. Dev. ED-23 pp 196-200, Feb (1976).

16. White, M. H.; Lampe, D. R.; Blaha, F. C.; Mack, I. A., "Characterization of Surface Channel CCD Imaging Arrays at Low Light Levels" IEEE J. of Solid State Circuits SC-9 pp 1-13, Feb (1974).

17. Brodersen, R. W.; Emmons, S. P., "Noise in Buried Channel Charge Coupled Devices" IEEE Trans. on Elect Dev ED-23 pp 215-223, Feb (1976).

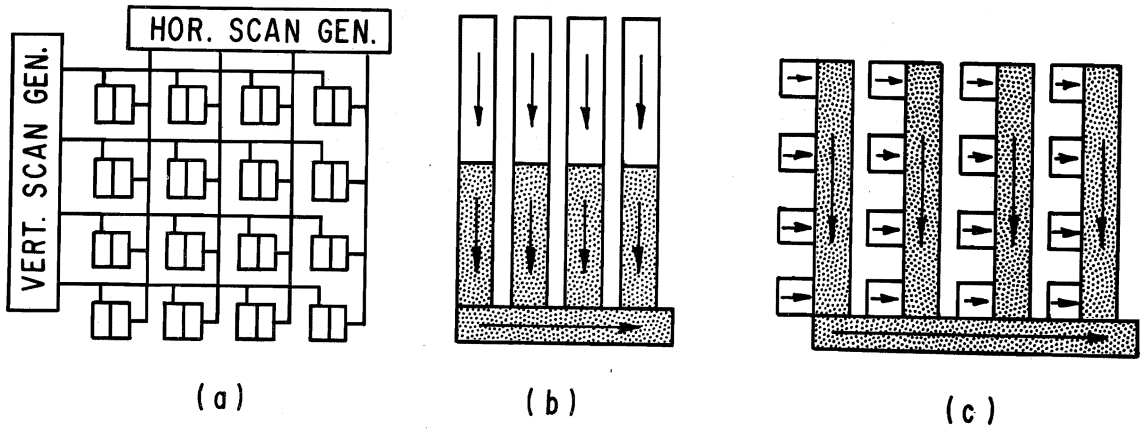

Fig. 1 - A Schematic of the (a) CID architecture, (b) the CCD frame transfer architecture and (c) the CCD interline transfer architecture.

Fig. 2 - Photo of the display from a 190 x 244 CID imager with a 1000X overload.

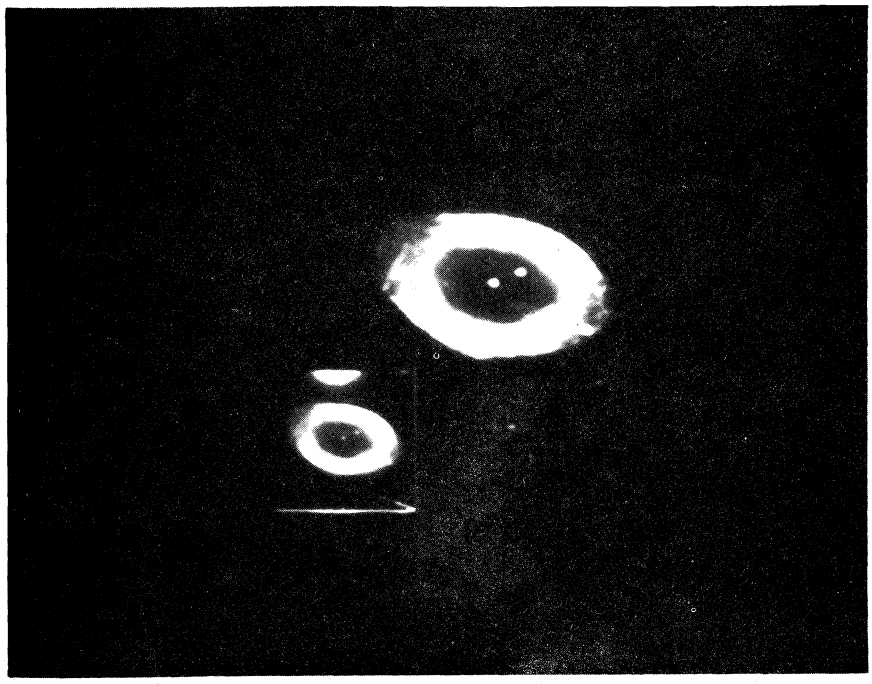

Fig. 3 - Photo of Ring Nebula in Lyra obtained with a CID imager at the Kitt Peak National Observatory

Fig. 4 - Further evaluation is required with this 244 x 248 CID imager.