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Digital Transmission Standard For Cable Television

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1 Introduction

This standard describes the framing structure, channel coding, and channel modulation for a digital multi-service television distribution system that is specific to a cable channel. The system can be used transparently with the distribution from a satellite channel, as many cable systems are fed directly from satellite links. The specification covers both 64 and 256 QAM. Most features of both modulation schemes are the same. Where there are differences, the specific details for each modulation scheme is covered.

The design of the modulation, interleaving and coding is based upon testing and characterization of cable systems in North America. The modulation is Quadrature Amplitude Modulation with a 64 point signal constellation (64-QAM) and with a 256 point signal constellation (256-QAM), transmitter selectable. The forward error correction (FEC) is based on a concatenated coding approach that produces high coding gain at moderate complexity and overhead. Concatenated coding offers improved performance over a block code, at a similar overall complexity. The system FEC is optimized for quasi error free operation at a threshold output error event rate of one error event per 15 minutes.

The data format input to the modulation and coding is assumed to be MPEG-2 transport. However, the method used for MPEG synchronization is decoupled from FEC synchronization. For example, this enables the system to carry Asynchronous Transfer Mode (ATM) packets easily without interfering with ATM synchronization. In fact, ATM synchronization may be performed by defined ATM synchronization mechanisms.

There are two modes supported: Mode 1 has a symbol rate of 5.057 Msps and Mode 2 has a symbol rate of 5.361 Msps. Typically, Mode 1 will be used for 64-QAM and Mode 2 will be used for 256-QAM. The system will be compatible with future implementations of higher data rate schemes employing higher order QAM extensions.

2 Symbols and abbreviations

2.1 SYMBOLS

For the purposes of this Recommendation, the following symbols are used:

α	Roll-off factor
byte	Eight bits
bps	Bits per second
g(x)	RS code generator polynomial
ms	millisecond
p(x)	RS field generator polynomial
q	Number of bits: 2,3,4 for 16-QAM, 32-QAM, 64-QAM, respectively
T	Number of bytes which can be corrected in RS error-protected packet

2.2 ABBREVIATIONS

For the purposes of this Recommendation, the following abbreviations are used:

ATM	Asynchronous Transfer Mode
FEC	Forward Error Correction
HEC	Header Error Control
HEX	Hexadecimal
LSB	Least Significant Bit
MPEG	Motion Picture Expert-Group
MSB	Most Significant Bit

PN	Pseudo Noise
ppm	Parts per million
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RS	Reed-Solomon
SNR	Signal to Noise Ratio
sps	Symbols per second

3 Cable system concept

Channel coding and transmission are specific to a particular medium or communication channel. The expected channel error statistics and distortion characteristics are critical in determining the appropriate error correction and demodulation. The cable channel, including optical fiber, is primarily regarded as a bandwidth-limited linear channel, with an optimized counterbalancing of various attenuation sources including: white noise, interference, and multi-path distortion. The Quadrature Amplitude Modulation (QAM) technique used, together with adaptive equalization and concatenated coding is well suited to this application and channel.

The basic layered block diagram of cable transmission processing is shown in Figure 1. The following sections define these layers from the “outside” in, and from the perspective of the transmit side.

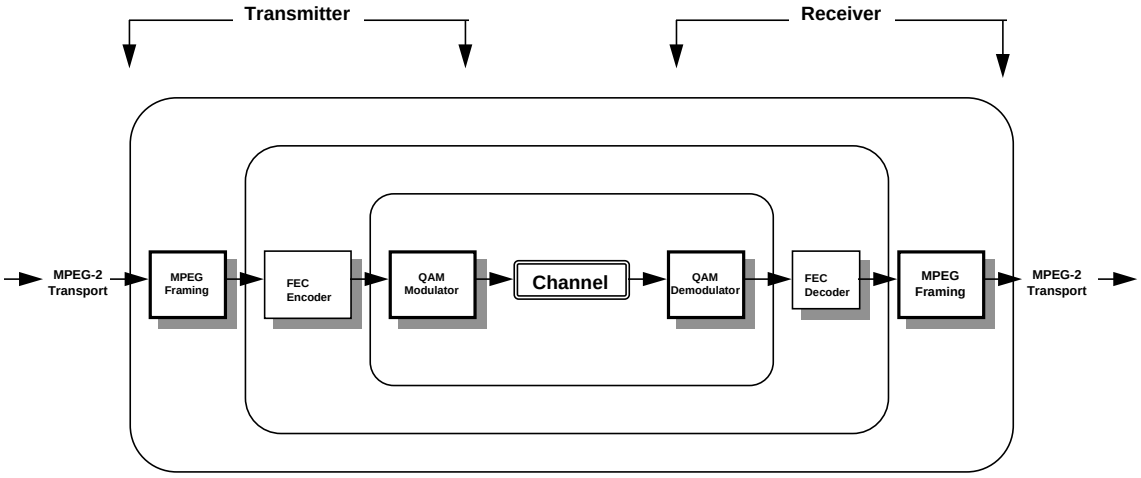


Figure 1 Cable transmission block diagram

4 MPEG-2 transport framing

The MPEG-2 transport layer is defined in Reference [1]. The transport layer for MPEG-2 data is comprised of packets having 188 bytes, with one byte for synchronization purposes, three bytes of header containing service identification, scrambling and control information, followed by 184 bytes of MPEG-2 or auxiliary data.

The MPEG transport framing is the outermost layer of processing. It is provided as a robust means of delivering MPEG packet synchronization to the receiver output. This processing block receives an MPEG-2 transport data stream consisting of a continuous stream of fixed length 188 byte packets. This data stream is transmitted in serial fashion, MSB first. The first byte of a packet is specified to be a sync byte having a constant value of 47_{HEX}.

The sync byte is intended for the purpose of packet delineation. The cable transmission system has incorporated an additional layer of processing to provide an additional functionality by utilizing the information bearing capacity of this sync byte. A parity checksum which is a coset of an FIR parity check linear block code is substituted for this sync byte, supplying improved packet delineation functionality, and error detection capability independent of the FEC layer.

The parity checksum is computed over the adjacent 187 bytes, which constitute the immediately preceding MPEG-2 packet contents (minus sync byte). It is then possible to support simultaneous packet synchronization and error detection. The decoder computes a sliding checksum on the serial data stream, using the detection of a valid code word to detect the start of a packet. Once a locked alignment condition is established, the absence of a valid code word at the expected location will indicate a packet error. The error flag of the previous packet may optionally be set as the data is passed out of the decoder. The normal sync word must be re-inserted in place of the checksum to provide a standard MPEG-2 data stream as an output.

The checksum is computed by passing the 1496 payload bits through a linear feedback shift register (LFSR) as described by the following equation:

$$f(X) = [1 + X^{1497}b(X)]/g(X), \text{ where } g(X) = 1 + X + X^5 + X^6 + X^8 \text{ and } b(X) = 1 + X + X^3 + X^7.$$

This computational structure is illustrated in Figures 2 and 3. All addition operations are assumed to be modulo 2. For an encode operation, the LFSR is first initialized so that all memory elements contain zero value. The 1496 bits which constitute the MPEG-2 transport stream packet payload are then shifted into the LFSR. The encoder input is set to zero after the 1496 data bits are received, and eight additional shifts are required to sequentially output the eight computed syndrome bits. This 8-bit result must then be passed through an additional FIR filtering function g(x) (initialized to an all-zeros state prior to introduction of the 8 syndrome bits) to generate an encoder checksum. An offset of 67_{HEX} is added to this checksum result for improved autocorrelation properties, and causes a 47_{HEX} result to be produced during a syndrome decode operation when a valid code word is present. The final 8-bit checksum with added offset is transmitted MSB first following the 1496 payload bits to implement a systematic encoder.

A parity check matrix may be used by the decoder to identify a valid checksum. A checksum generator as shown in Figure 3 with an offset of zero may be employed for this purpose. The code has been designed such that when the appropriate 188 bytes of the modified MPEG-2 transport stream packet (which includes the associated checksum) are multiplied with the parity check matrix, a valid code word is indicated when the calculated product produces a 47_{HEX} result. Each of the 8 columns of the parity check matrix "P" includes a 1497 bit vector, hereafter referred to as "C". This vector is defined in Figure 4.

As you proceed from the leftmost column of the matrix "P", the 1497-bit column "C" is duplicated in subsequent columns of the matrix "P", shifted down by one bit position. The bit positions unoccupied by the column data are filled with zeros, as illustrated in Figure 5.

Note that the checksum is calculated based on the previous 187 bytes and not the 187 bytes yet to be received by the MPEG-2 sync decoder. This is in contrast to the conventional notion of an MPEG packet structure, in that the sync byte is usually described as the first byte of a received packet.

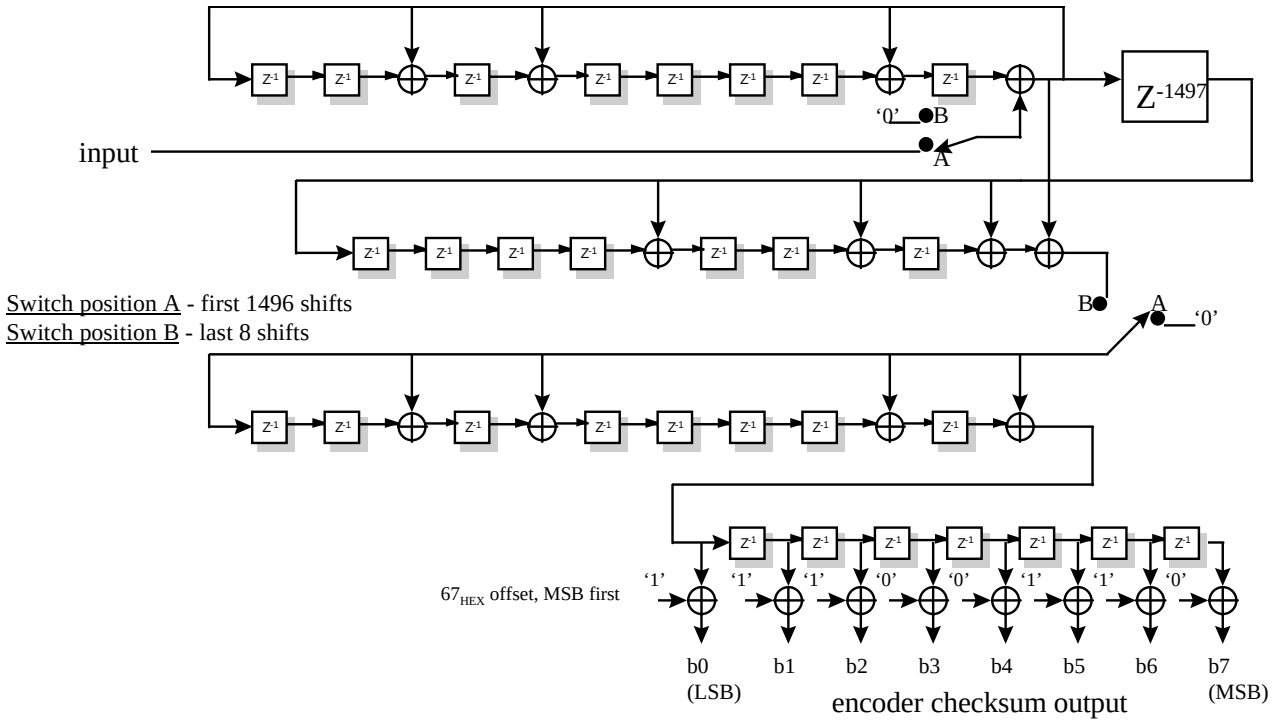


Figure 2 Checksum generator for the MPEG-2 sync byte encoder

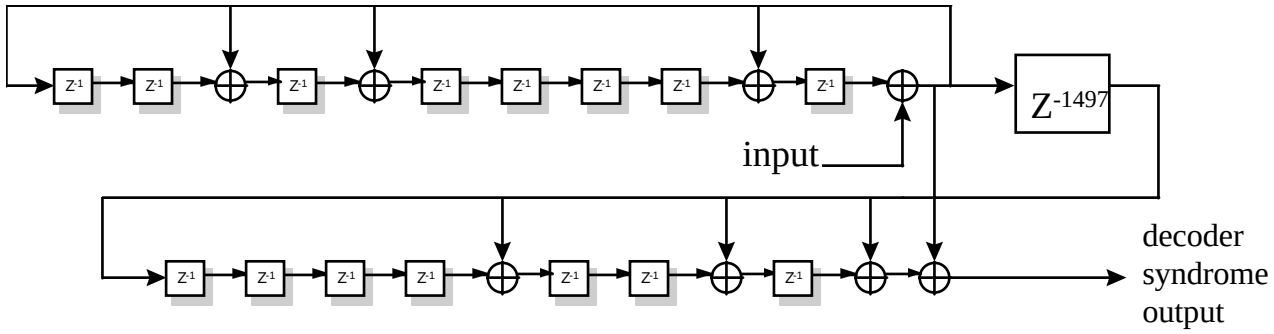


Figure 3 Syndrome generator for the MPEG-2 sync decoder

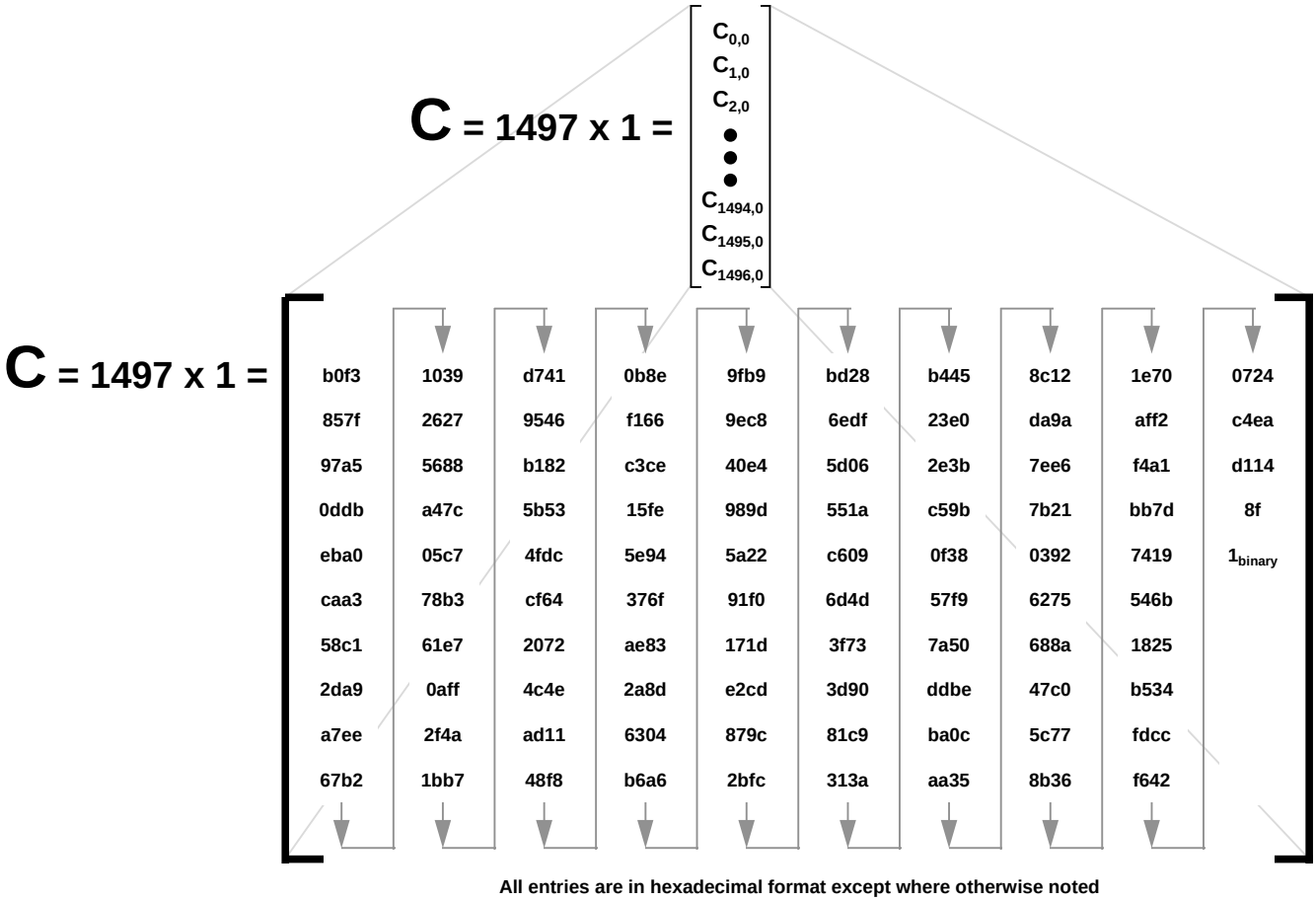


Figure 4 "C" column vector (replicated inside the parity check matrix)

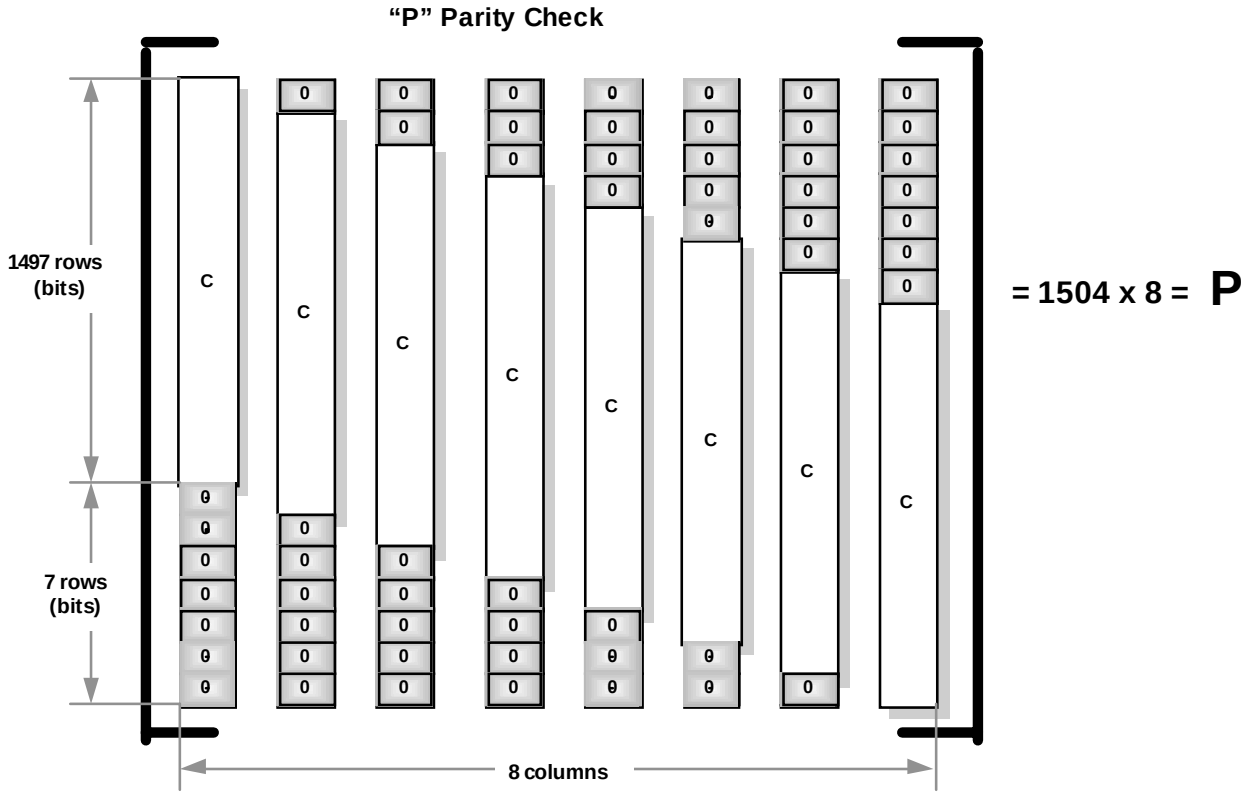


Figure 5 - Structure of the parity check matrix "P"

The received vector "R" is the MPEG-2 data consisting of 187 bytes followed by the checksum byte, yielding a total of 1504 bits. This "R" vector is multiplied (modulo 2) by the parity check "P" matrix, yielding an "S" vector whose length is 8-bits, as illustrated in Figure 6.

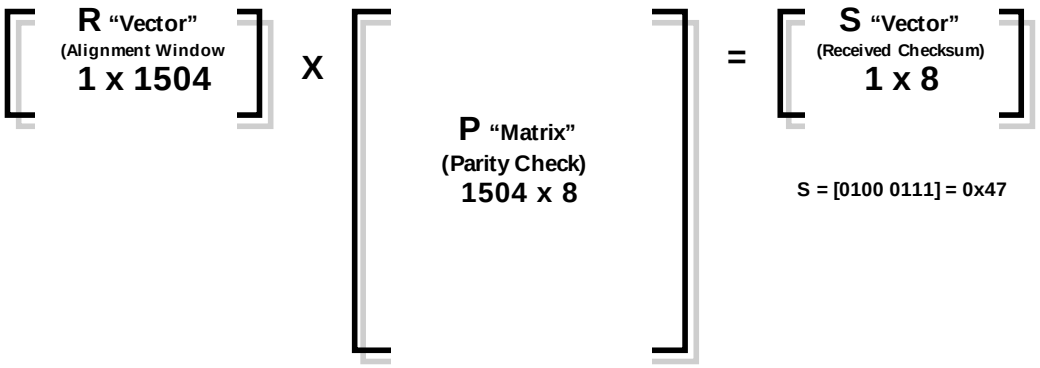


Figure 6 Received MPEG-2 vector and parity check matrix multiplication

A valid checksum is indicated when **S = [0100, 0111] = 47_{HEX}.**

For carriage of transport protocols other than MPEG-2 Transport, e.g., ATM, this outer layer is removed or bypassed. The FEC layer accepts and delivers data without any constraints on protocol. The framing section could be replaced with one appropriate to the alternative transport protocol if required by an application. All other portions of this specification (modulation, coding, interleaving) are implemented as described below. For the case of ATM, no framing layer is required. The ATM Header Error Control byte (HEC) typically provides adequate packet framing and error detection. Isochronous ATM streams are therefore carried transparently without overhead for MPEG or quasi-MPEG packet encapsulation.

5 Forward error correction

The forward error correction (FEC) definition is composed of four processing layers, as illustrated in Figure 7. There are no dependencies on input data protocol in any of the FEC layers. FEC synchronization is fully internal and transparent. Any data sequence will be delivered from the encoder input to decoder output.

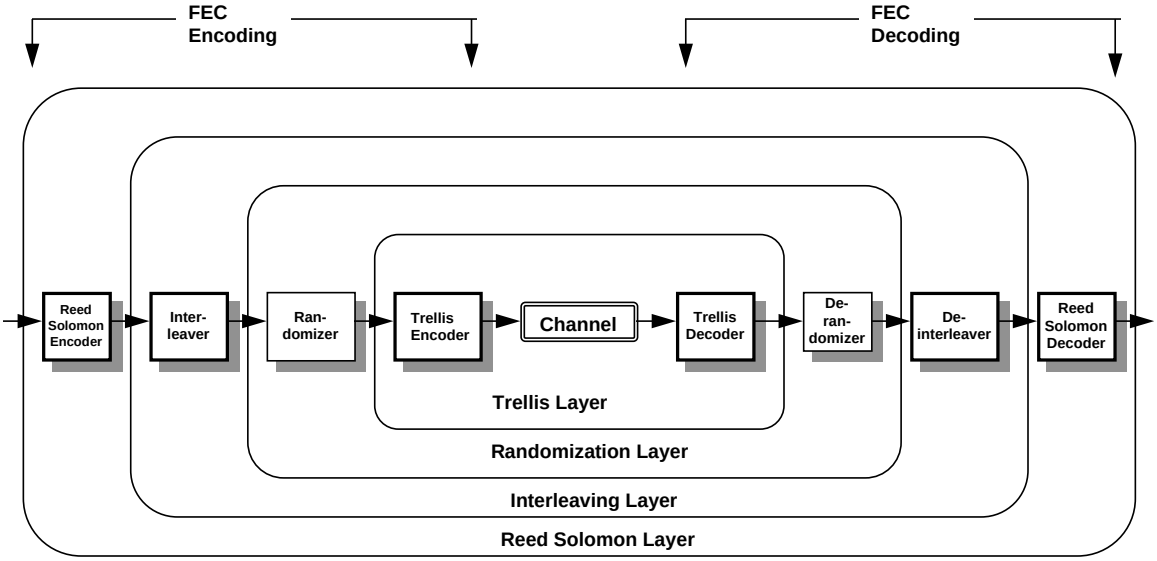


Figure 7 Layers of processing in the FEC

The FEC section uses various types of error correcting algorithms and interleaving techniques to transport data reliably over the cable channel.

Reed-Solomon (R-S) Coding – Provides block encoding and decoding to correct up to three symbols within an R-S block.

Interleaving – Evenly disperses the symbols, protecting against a burst of symbol errors from being sent to the R-S decoder.

Randomization – Randomizes the data on the channel to allow effective QAM demodulator synchronization.

Trellis Coding – Provides convolutional encoding and with the possibility of using soft decision trellis decoding of random channel errors.

The following subsections define these 4 layers.

5.1 REED-SOLOMON CODING

The MPEG-2 transport stream is Reed-Solomon (R-S) encoded using a (128,122) code over GF(128). This code has the capability of correcting up to t=3 symbol errors per R-S block. The same R-S code is used for both 64-QAM and 256-QAM. However, the FEC frame format is different for each modulation type, as described in a later section.

The Reed-Solomon encoder implementation is described in this subsection. A systematic encoder is utilized to implement a t=3, (128,122) extended Reed-Solomon code over GF(128). The primitive polynomial used to form the field over GF(128) is:

$$P(X) = X^7 + X^3 + 1$$

where $P(\alpha) = 0$.

The generator polynomial used by the encoder is:

$$g(X) = (X+\alpha)(X+\alpha^2)(X+\alpha^3)(X+\alpha^4)(X+\alpha^5)$$

$$= X^5 + \alpha^{52}X^4 + \alpha^{116}X^3 + \alpha^{119}X^2 + \alpha^{61}X + \alpha^{15}$$

The message polynomial input to the encoder consists of 122, 7-bit symbols, and is described below:

$$m(X) = m_{121}X^{121} + m_{120}X^{120} + \ldots m_1X + m_0$$

This message polynomial is first multiplied by X^5, then divided by the generator polynomial g(X) to form a remainder, described by the following:

$$r(X) = r_4X^4 + r_3X^3 + r_2X^2 + r_1X + r_0$$

This remainder constitutes five parity symbols which are then added to the message polynomial to form a 127 symbol code word that is an even multiple of the generator polynomial.

The generated code word is now described by the following polynomial:

$$c(X) = m_{121}X^{126} + m_{120}X^{125} + m_{119}X^{124} + \ldots + r_4X^4 + r_3X^3 + r_2X^2 + r_1X + r_0$$

A valid code word will have roots at the first through fifth powers of α.

An extended parity symbol (c_) is generated by evaluating the code word at the sixth power of α.

$$c\_ = c(\alpha^6)$$

This extended symbol is used to form the last symbol of a transmitted Reed-Solomon block. The extended code word then appears as follows:

$$\hat{c} = Xc(X) + c\_$$
$$= m_{121}X^{127} + m_{120}X^{126} + \ldots + m_1X^7 + m_0X^6 + r_4X^5 + r_3X^4 + r_2X^3 + r_1X^2 + r_0X + c\_$$

The structure of a Reed-Solomon block which illustrates the order of transmitted symbols output from the R-S encoder is shown below:

$m_{121}m_{120}m_{119}\ldots m_1m_0r_4r_3r_2r_1r_0c\_$ (order sent is left to right)

5.2 INTERLEAVING

Interleaving is included in the modem between the R-S block coding and the randomizer to enable the correction of burst noise induced errors. In both 64-QAM and 256-QAM a convolutional interleaver is employed. The interleaver consists of a single fixed structure for the nominal 64-QAM (level 1), and a programmable structure for both 64-QAM and 256-QAM (level 2).

Convolutional interleaving is illustrated in Figure 8. At the start of an FEC frame defined in a subsequent section, the interleaving commutator position is initialized to the top-most branch and increments at the R-S symbol frequency, with a single symbol output from each position. With a convolutional interleaver the R-S code symbols are sequentially shifted into the bank of 128 registers (the width of each register is 7 bits which matches the R-S symbol size). Each successive register has J symbols more storage than the preceding register. The first interleaver path has zero delay, the second has a J symbol period of delay, the third 2*J symbol periods of delay, and so on, up to the I^{th} path which has (I-1)*J symbol periods of delay. This is reversed for the de-interleaver in the Cable Decoder such that the net delay of each R-S symbol is the same through the interleaver and de-interleaver. Burst noise in the channel causes a series of bad symbols. These are spread over many R-S blocks by the de-interleaver such that the resultant symbol errors per block are within the range of the R-S decoder correction capability.

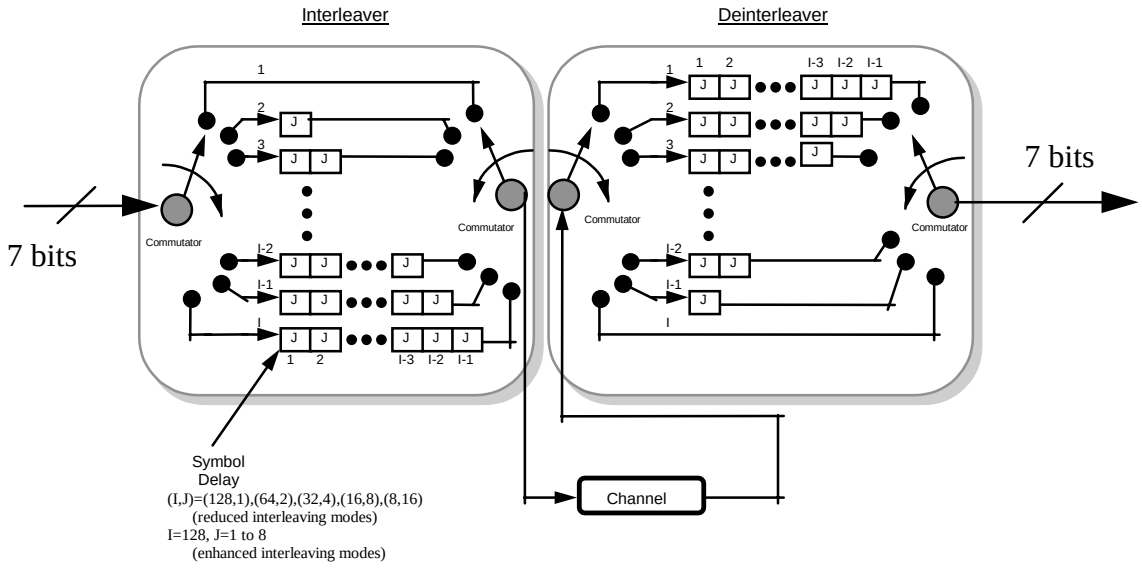


Figure 8 Interleaving functional block diagram

With regard to interleaving capability, two distinct operating modes are specified, hereafter referred to as *level 1* and *level 2*.

Level 1 is specified for 64-QAM transmission only. This mode accommodates the installed base of legacy 64-QAM-only digital set tops. While operating in level 1, a single interleaving depth will be supported; namely I=128, J=1.

Level 2 shall encompass 64-QAM and 256-QAM transmission, and will for both modulation schemes be capable of supporting variable interleaving. This will include both enlarged and reduced interleaving depths relative to the nominal 64-QAM (level 1) configuration. Four data bits are transmitted in-band during the FEC frame sync interval to convey the interleaving parameters to the receiver for a given channel.

Table 1 describes the interleaver parameters for level 1 operation, with associated latency and burst protection. Table 2 describes the decoding of the 4-bit in band control word into the I and J interleaving parameters for level 2 operation, also with associated burst protection and latency.

Table 1 Level 1 Interleaving

Control Word (4 bits)	I(# of taps)	J(increment)	Burst Protection	Latency
XXXX	128	1	95µs	4.0ms

Table 2 Level 2 Interleaving

Control Word (4 bits)	I(# of taps)	J(increment)	Burst Protection 64QAM/256QAM	Latency 64QAM/256QAM
0001	128	1	95µs/66µs	4.0ms/2.8ms
0011	64	2	47µs/33µs	2.0ms/1.4ms
0101	32	4	24µs/16µs	0.98ms/0.68ms
0111	16	8	12µs/8.2µs	0.48ms/0.33ms
1001	8	16	5.9µs/4.1µs	0.22ms/0.15ms
1011	reserved			
1101	reserved			
1111	reserved			
0000	128	1	95µs/66µs	4.0ms/2.8ms
0010	128	2	190µs/132µs	8.0ms/5.6ms
0100	128	3	285µs/198µs	12ms/8.4ms
0110	128	4	379µs/264µs	16ms/11ms

5.3 FRAME SYNCHRONIZATION SEQUENCE

The frame synchronization sequence trailer delineates the FEC frame, providing synchronized R-S coding, interleaving, and randomization. Additionally, trellis groups for 256-QAM only are aligned with the FEC frame. The FEC framing does not perform MPEG packet or trellis decoder synchronization. The R-S block and 7-bit symbol structures are aligned with the end of the frame for both 64 and 256-QAM.

For 64-QAM, an FEC frame consists of a 42 bit sync trailer which is appended to the end of 60 R-S blocks, with each R-S block containing 128 symbols. Each R-S symbol consists of 7-bits. Thus, there is a total of 53,760 data bits and 42 frame sync trailer bits in this FEC frame. The first 4 7-bit symbols of the frame sync trailer contain the 28-bit "unique" synchronization pattern (1110101 0101100 0001101 1101100) or $(75\ 2C\ 0D\ 6C)_{HEX}$. The remaining 2 symbols (14 bits) are utilized as follows: first 4 bits for interleaver mode control, and 10 bits are reserved and set to zero. The frame sync trailer is inserted by the encoder and detected at the decoder. The decoder circuits search for this pattern and determine the location of the frame boundary and interleaver depth mode when found. The FEC frame for 64-QAM is shown in Figure 9.

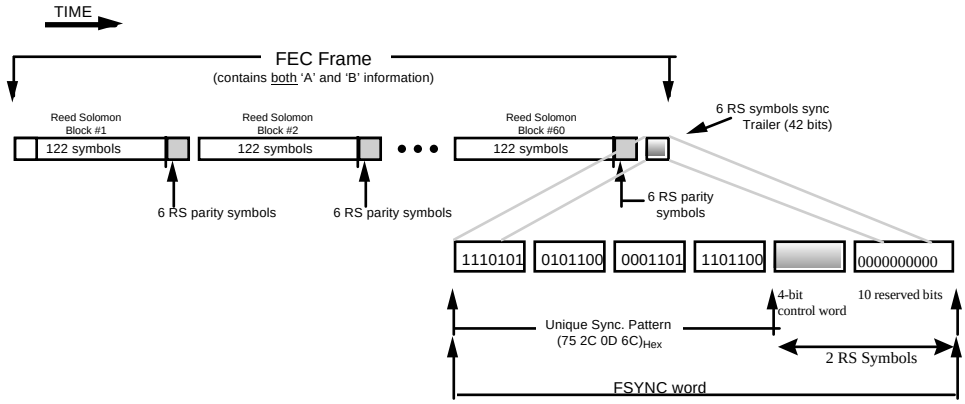


Figure 9 Frame packet format for 64-QAM

For 256-QAM, an FEC frame consists of a 40 bit sync trailer which is appended to the end of 88 R-S blocks, with each R-S block containing 128 symbols. Each R-S symbol consists of 7 bits. Thus, there is a total of 78,848 data bits and 40 frame sync trailer bits in this FEC frame. The 40 bit frame sync trailer is divided as follows: 32 bits are the "unique" synchronization pattern (0111 0001 1110 1000 0100 1101 1101 0100) or $(71\ E8\ 4D\ D4\ )_{HEX}$, 4 bits are a control word which determine the size of the interleaver employed, and 4 bits are a reserved word which is set to zero. The FEC frame for 256-QAM is shown in Figure 10.

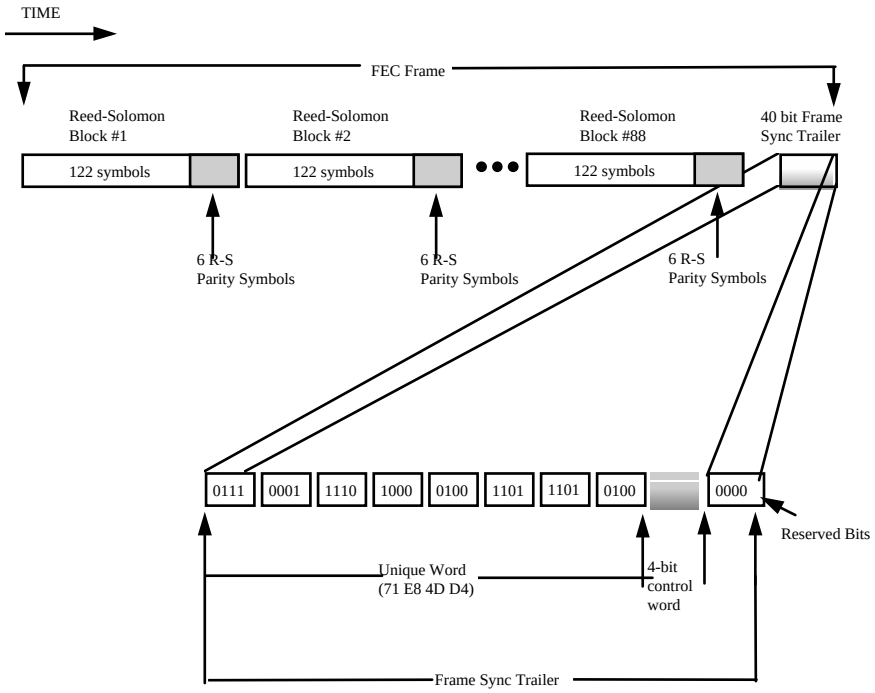


Figure 10 Frame packet format for 256-QAM

Note that there is no synchronization relationship between the transmitted R-S block and transport data packets. Thus, MPEG-2 transport stream packet synchronization is obtained independently from R-S frame synchronization. This keeps the FEC and transport layers decoupled and independent.

5.4 RANDOMIZATION

The randomizer shown in Figure 11 is the third layer of processing in the FEC block diagram. The randomizer provides for even distribution of the symbols in the constellation, which enables the demodulator to maintain proper lock. The randomizer adds a pseudorandom noise (PN) sequence of 7 bit symbols over GF(128) (i.e. bit-wise exclusive-OR) to the symbols within the FEC frame to assure a random transmitted sequence.

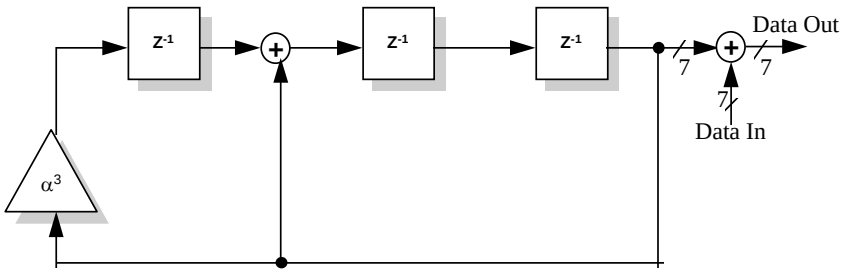
For both 64 and 256-QAM, the randomizer is initialized during the FEC frame trailer, and is enabled at the first symbol after the trailer. Thus the trailer itself is not randomized, and the initialized output value randomizes the first data symbol.

Initialization is defined as preloading to the 'all ones' state for the randomizer structure shown in Figure 11. The randomizer uses a linear feedback shift register specified by a GF(128) polynomial defined as follows:

$$f(x) = x^3 + x + \alpha^3$$

where

$$\alpha^7 + \alpha^3 + 1 = 0.$$



The Randomizer Polynomial

$$f(x) = x^3 + x + \alpha^3$$

Figure 11 Randomizer (7-bit symbol scrambler)

5.5 TRELLIS CODED MODULATION

As part of the concatenated coding scheme, trellis coding is employed for the inner code. It allows the introduction of redundancy to improve the threshold signal-to-noise ratio (SNR) by increasing the symbol constellation without increasing the symbol rate. As such, it is more properly termed "trellis coded modulation".

64-QAM Modulation Mode

For 64-QAM, the input to the trellis coded modulator is a 28 bit sequence of four, 7 bit R-S symbols, which are labeled in pairs of 'A' symbols and 'B' symbols. A block diagram of a 64-QAM trellis coded modulator is shown in Figure 12. All 28 bits are assigned to a trellis group, where each trellis group forms 5 QAM symbols, as shown in Figure 13.

Of the 28 input bits that form a trellis group, each of two groups of 4 bits of the differentially precoded bit streams in a trellis group are separately encoded by a binary convolutional coder (BCC). Each BCC produces 5 coded bits, as shown in Figure 12. The remaining bits are sent to the mapper uncoded. This will produce an overall output of 30 bits. Thus, the overall code rate for 64-QAM trellis coded modulation is 14/15.

The trellis group is formed from R-S symbols as follows: For the "A" symbols, the R-S symbols are read, from MSB to LSB, A_{10} , A_8 , A_7 , A_5 , A_4 , A_2 , A_1 and A_9 , A_6 , A_3 , A_0 , A_{13} , A_{12} , A_{11} . The four MSB's of the second symbol are input to the BCC, one bit at a time, LSB first. The remaining bits of the second symbol and all the bits of the first symbol are input to the mapper, uncoded, LSB first one bit at a time. The four bits sent to the BCC will produce 5 coded bits labeled U_1 , U_2 , U_3 , U_4 , U_5 . The same process is done for the "B" bits. The process can be seen in Figure 12. With 64-QAM, 4 R-S symbols conveniently fit into one trellis group, and in this case the sync word may occupy every bit position within a trellis group.

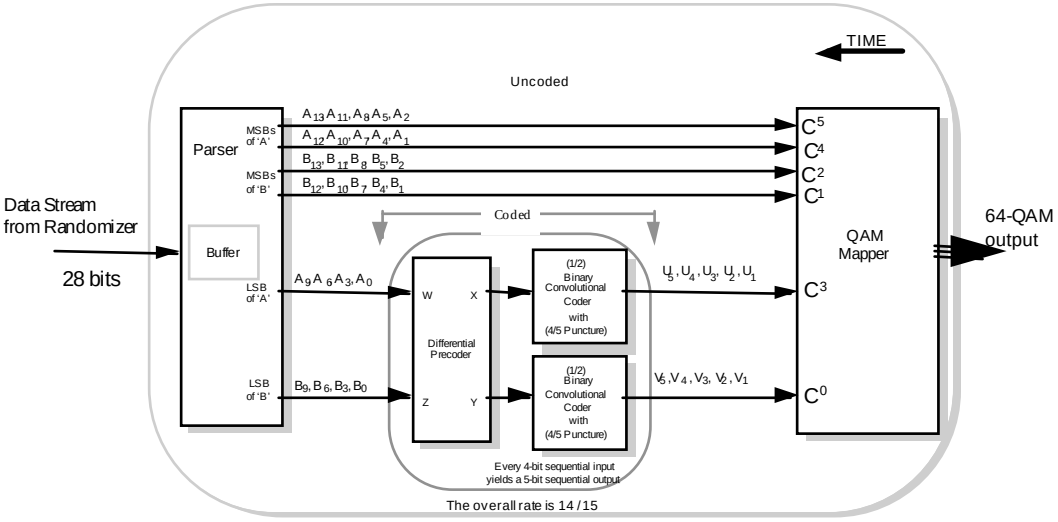
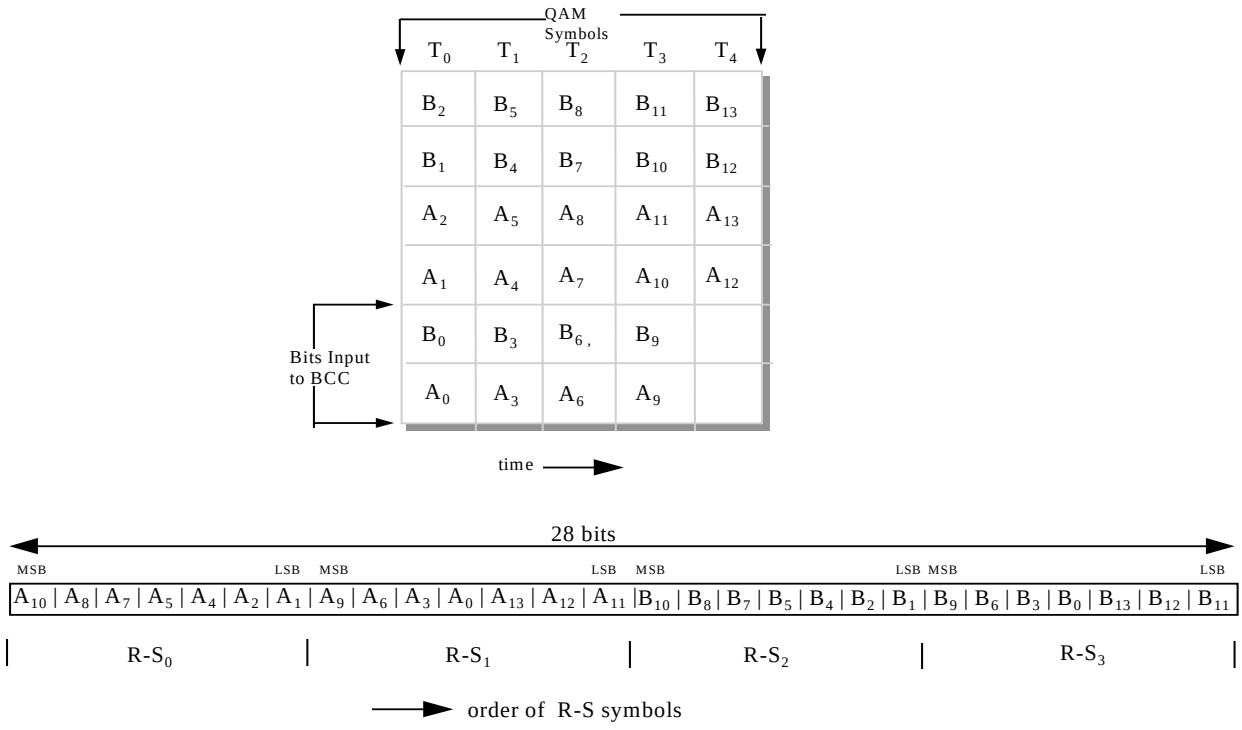


Figure 12 64-QAM trellis coded modulator block diagram



R-S symbol to Trellis Group bit ordering

Figure 13 64-QAM trellis group

256-QAM Modulation Mode

For 256-QAM, an analogous trellis coding is employed using the same BCC as 64-QAM, with the same rate 1/2 generator and the same 4/5 puncture matrix. The 256-QAM trellis coded modulator is shown in Figure 14. In this case all the FEC frame sync information is embedded only in the convolutionally encoded bit positions of a trellis group, as shown in Figure 15.

There are two distinct types of trellis groups in 256-QAM: hereafter referred to as a *non-sync group* and a *sync group*. Each trellis group generates 5 QAM symbols at the modulator, the non-sync group contains 38 data bits while the sync group contains 30 data bits and 8 sync bits. Figure 15 shows both a non-sync trellis group and a sync trellis group. Since there are 88 R-S blocks plus 40 frame sync bits per FEC frame, there will be a total of 2,076 trellis groups per frame. Of these trellis groups, 2,071 are non-sync trellis groups and 5 are sync trellis groups. The 5 sync trellis groups come at the end of the frame. The frame sync trailer is aligned to the trellis groups. In the encoder, the trellis group is further divided into two groups: one uncoded bit stream and one coded bit stream. The MSB of the first R-S symbol in the FEC frame is assigned to the first bit in the first non-sync trellis group, as shown in the ordering in Figure 15. The output from each BCC is the five parity bits labeled U_1 through U_5 and V_1 through V_5, respectively, as shown in Figure 14.

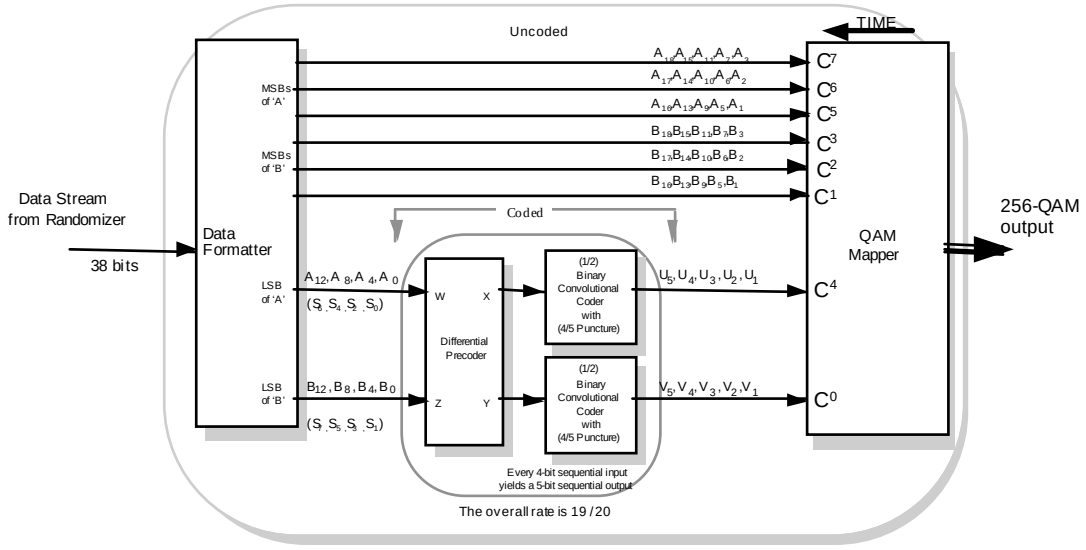


Figure 14 256-QAM trellis coded modulator block diagram

To form trellis groups from R-S code words, the R-S code words are serialized beginning with the MSB of the first symbol of the first R-S code word following the frame sync trailer. Bits are placed into trellis group locations from R-S symbols in the order: A_0 B_0 A_1 ... B_3 A_4 B_4 ... B_{16} B_{17} B_{18} as shown in Figure 15. For sync trellis groups, the bits from serialized R-S symbols are placed beginning at location A_1 instead of A_0. The last five trellis groups in an FEC frame each contains 8 of the 40 sync bits, S_0 S_1...S_7 in the frame sync trailer shown in Figure 10.

Of the 38 input bits that form a trellis group, each of two groups of 4 bits of the differentially precoded bit streams in a trellis group isseparately encoded by a binary convolutional coder (BCC). Each BCC produces 5 coded bits, as shown in Figure 14. The remaining bits are sent to the QAM mapper uncoded. This produces a total output of 40 bits per trellis group. Thus, the overall code rate for 256-QAM trellis coded modulation is 19/20.

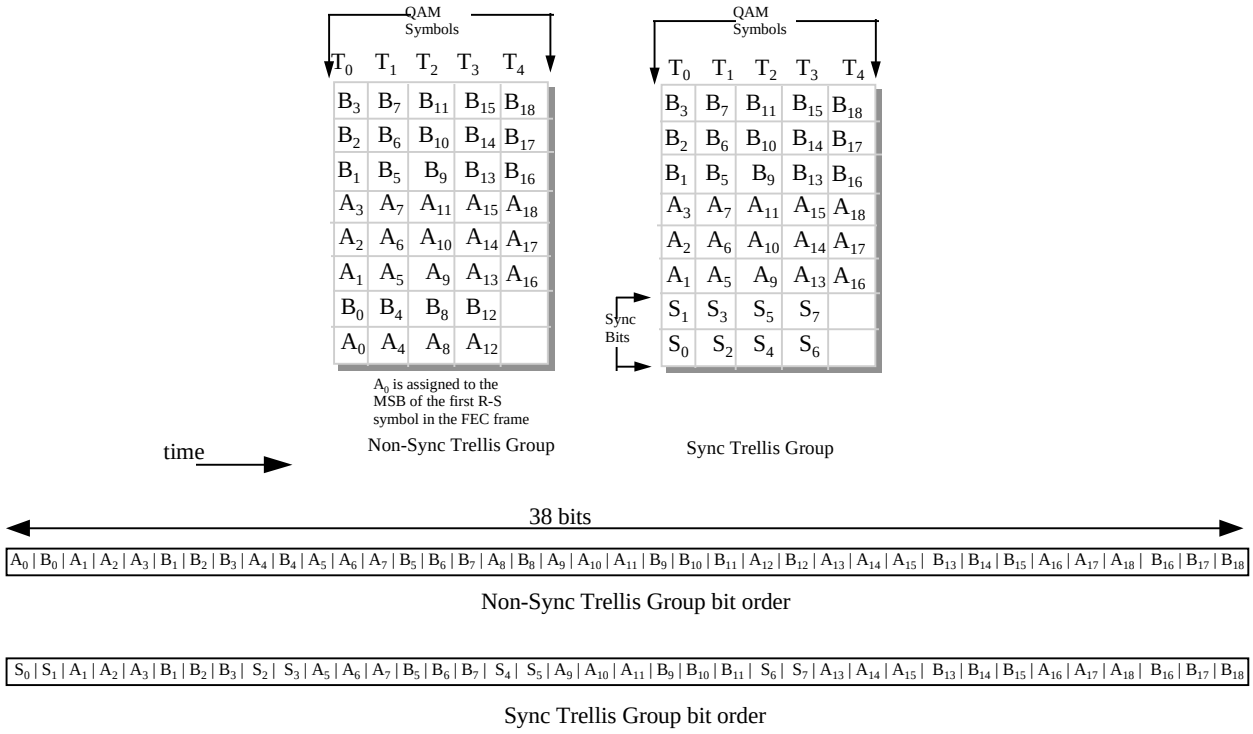
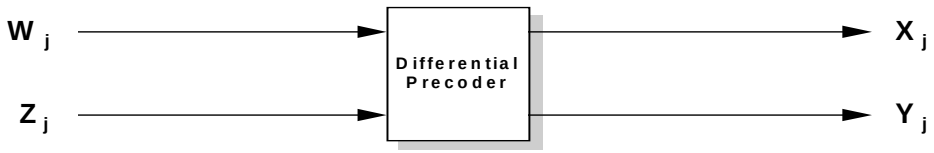


Figure 15 256-QAM sync and non-sync trellis groups

Rotationally Invariant Pre-coding

The differential precoder shown in Figure 16 performs the 90° rotationally invariant trellis coding. Rotationally invariant coding is employed for both 64 and 256-QAM modulation. The key for robust modem design is to have very fast recovery from carrier phase slips**.** Non-rotationally invariant coding would require re-synchronization of the FEC when the carrier phase tracking changes quadrant alignment, leading to a burst of errors at the FEC output.

The differential precoder allows the information to be carried by the change in phase, rather than by the absolute phase. For 64-QAM, the 3rd and the 6th bits of the 6-bit symbols are differentially encoded, and for 256-QAM, the 4th and 8th bits are differentially encoded. If you mask out the 3rd and the 6th bits in 64-QAM as in Figure 18 (labeled C^3 and C^0) and the 4th and 8th bits in 256-QAM as in Figure 19 (labeled C^4 and C^0) the 90° rotational invariance of the remaining bits is inherent in the labeling of the symbol constellation.



Differential Precoder Equations

$$X_j = W_j + X_{j-1} + Z_j(X_{j-1} + Y_{j-1})$$

$$Y_j = Z_j + W_j + Y_{j-1} + Z_j(X_{j-1} + Y_{j-1})$$

Figure 16 Differential precoder

Binary Convolutional Coder

The trellis coded modulator includes a punctured rate 1/2 binary convolutional encoder that is used to introduce the redundancy into the LSB's of the trellis group. The convolutional encoder is a 16-state non-systematic rate 1/2 encoder with the generator: G1 = 010 101, G2 =011 111 ($25,37_{octal}$), or equivalently the generator matrix [$1 \oplus D^2 \oplus D^4$, $1 \oplus D \oplus D^2 \oplus D^3 \oplus D^4$]. At the beginning of a trellis group, the BCC commutator is initially in the G1 position. For each input bit presented to the tapped delay line, two bits (G1, followed by G2) are subsequently produced at the output in accordance with the associated set of generator coefficients. For each trellis group, four input bits produce eight convolutionally encoded bits. The time output of the encoder is selected according to a puncture matrix: [P1, P2] = [0001;1111] ("0" denotes NO transmission, "1" denotes transmission), which produces a single serial bit stream. The puncture matrix essentially converts the rate 1/2 encoder to rate 4/5, since only five of the eight encoded bits are retained after puncturing. The internal structure of the punctured encoder is illustrated in Figure 17.

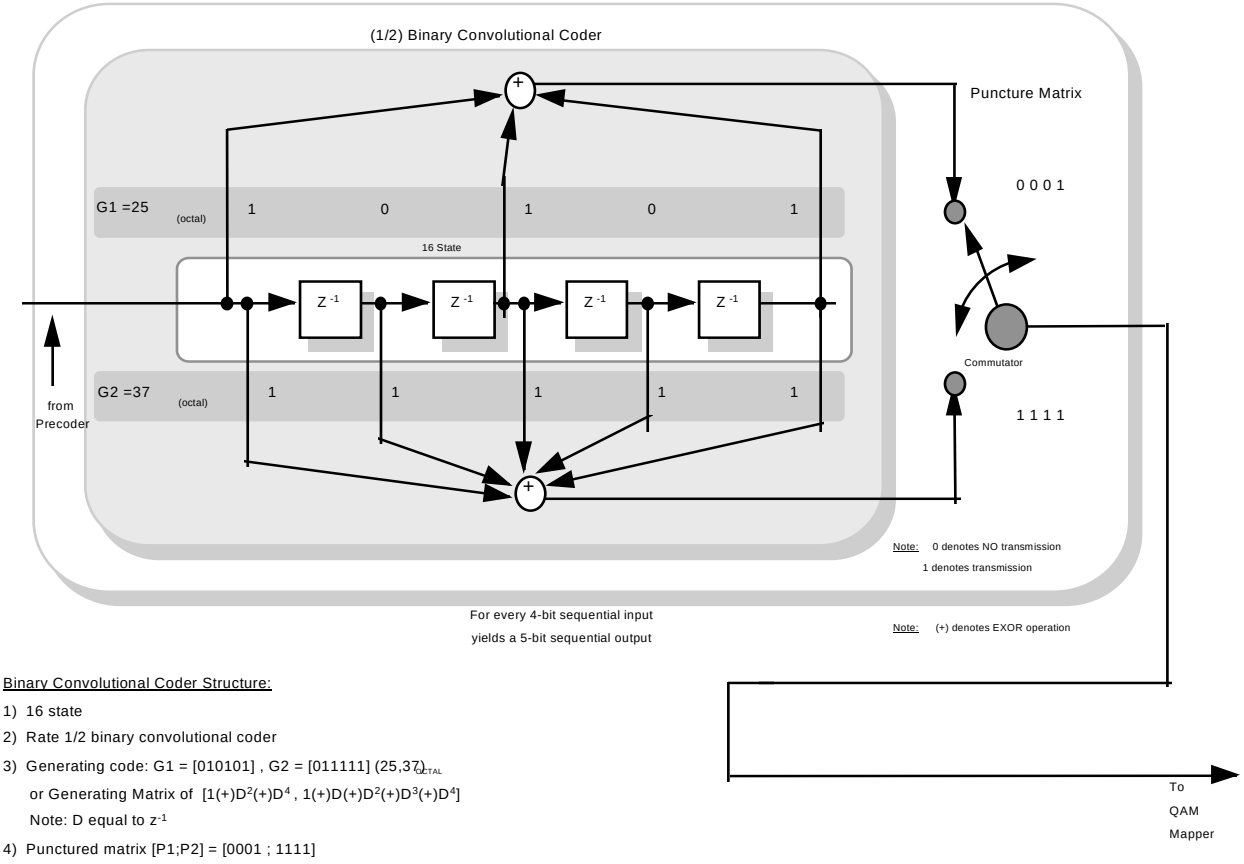


Figure 17 Punctured binary convolutional coder

QAM Constellation Mapping

For 64-QAM, the QAM mapper receives the coded and uncoded 3-bit **'**A' and 'B' data from the trellis coded modulator. It uses these bits to address a look-up table which produces the 6-bit constellation symbol. The 6-bit constellation symbol is then sent to the 64-QAM modulator where the signal constellation illustrated in Figure 18 is generated.

For 256-QAM, the QAM mapper receives the coded and uncoded 4-bit **'**A' and 'B' data from the trellis coded modulator. It uses these bits to address a look-up table which produces the 8-bit constellation symbol. The 8-bit constellation symbol is then sent to the 256-QAM modulator where the signal constellation illustrated in Figure 19 is generated.

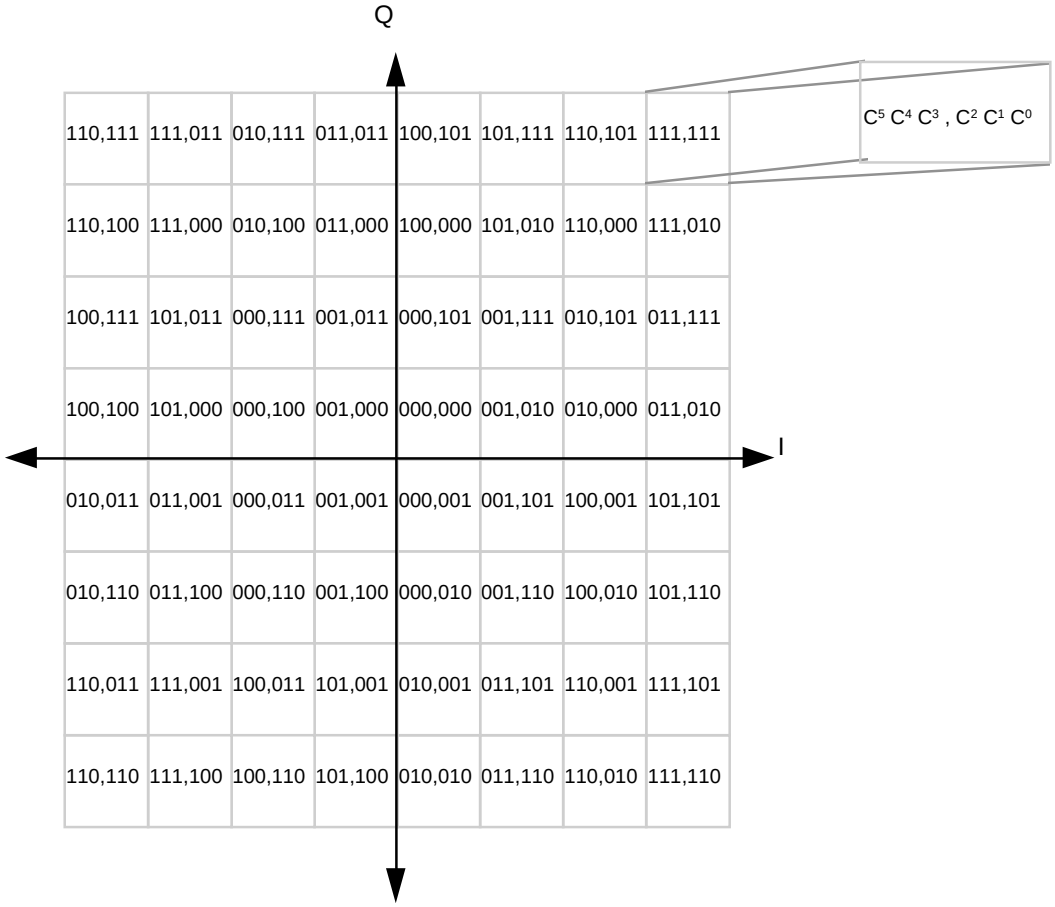


Figure 18 64-QAM constellation

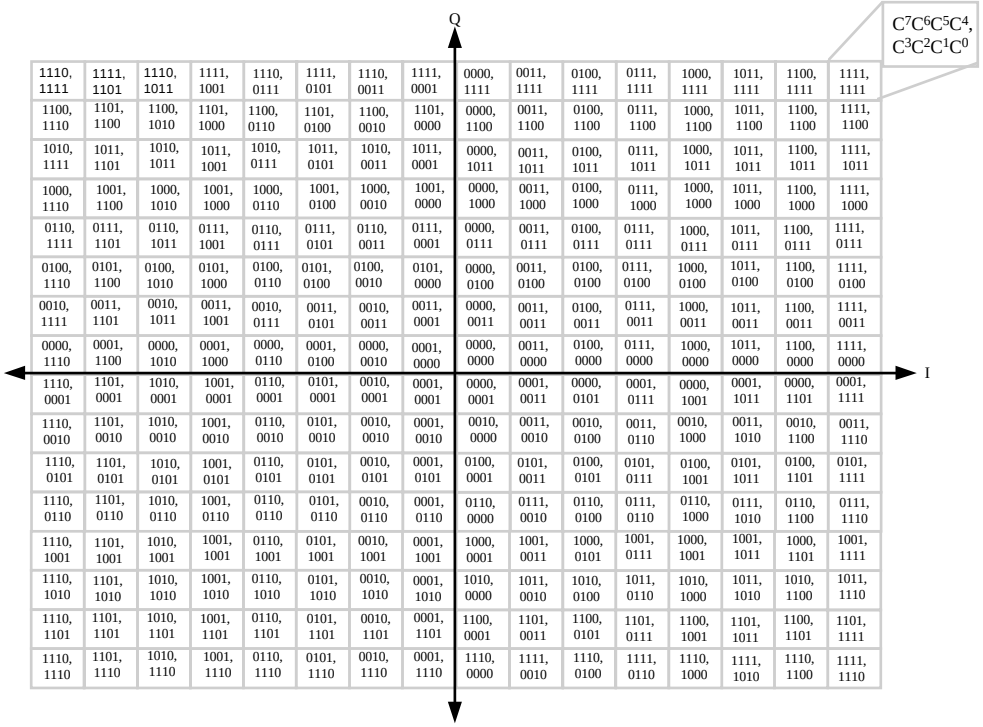


Figure 19 256-QAM constellation

6 Modulation and demodulation

6.1 QAM CHARACTERISTICS

The cable transmission format is summarized in Table 3 for 64-QAM and 256-QAM. Table 4 contains a summary of the pertinent characteristics of the variable interleaving modes.

TABLE 3 Cable transmission format

Parameter	64-QAM Format	256-QAM Format
Modulation	64 QAM, rotationally invariant coding	256 QAM, rotationally invariant coding
Symbol size	3-bits for "I" and 3 bits for "Q" dimensions	4-bits for "I" and 4 bits for "Q" dimensions
Transmission band	54 to 860 MHz[1]	54 to 860 MHz[1]
Channel spacing	6 MHz[1]	6 MHz[1]
Symbol rate	5.056941 Msps +/- 5 ppm[1]	5.360537 Msps +/- 5 ppm[1]
Information bit rate	26.97035 Mbps +/- 5 ppm[1]	38.81070 Mbps +/- 5 ppm[1]
Frequency response	Square root raised cosine filter (Roll-off ≈ 0.18)	Square root raised cosine filter (Roll-off ≈ 0.12)
FEC Framing	42 bit sync trailer following 60 R-S blocks (see 5.3)	40 bit sync trailer following 88 R-S blocks (see 5.3)
QAM Constellation Mapping	6 bits per symbol (see 5.5)	8 bits per symbol (see 5.5)

TABLE 4 Variable interleaving modes

	Level 1	Level 2
QAM format	64-QAM (see Table 3)	64 or 256-QAM (see Table 3)
Interleaving	Fixed interleaving (see 5.2) I=128 J=1	Variable interleaving (see 5.2) I=128,64,32,16,8 J=1,2,3,4,8,16

6.2 QAM MODULATOR RF OUTPUT

The RF modulated QAM signal s(t) is given by:

$$s(t) = I(t)\cdot\cos(2\pi ft) + Q(t)\cdot\sin(2\pi ft)$$

where t denotes time, f denotes RF carrier frequency and where I(t) and Q(t) are the respective Root-Nyquist filtered baseband quadrature components of the constellation symbols.

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[1]These values are specific to 6 MHz channel spacing. Additional sets of values for differing channel spacing are under study.

7 References

The following Recommendations and other references contain provisions which, through reference in the text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references

are subject to revision; all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of currently valid ITU-T Recommendations is regularly published.

[1] ITU-T Recommendation H.222.0 (2000) ISO/IEC 13818-1:2000, , Information technology- Generic coding of moving pictures and associated audio information: systems

ANNEX A
(INFORMATIVE)

CALCULATION OF CONCATENATED CODE RATE FOR QAM CABLE TRANSMISSION

As explained in Section 5, the forward error correction (FEC) definition is composed of a concatenated outer block code and an inner trellis code. A Reed-Solomon (R-S) block code with framing, interleaving, and randomization followed by trellis coded modulation (TCM) with differential pre-coding and punctured binary convolutional coding is used. This concatenated FEC coding definition produces an overall coding rate determined by the individual coding steps that expand the contents of the QAM channel symbols beyond the input user information. The overall coding rate that relates channel QAM symbol rate to the input information bit rate is derived as follows.

The outer block code consists of an R-S block code. In general, an R-S code is defined over a GF(2^m) finite field which carries K information symbols in an N symbol code word, where N is greater than K and each symbol consists of m bits. The input information rate to output coded rate ratio is defined as the code rate, which is less than or equal to one. Hence, the additional redundancy of the N-K syndrome symbols incurs a rate loss through the R-S code, defined as the R-S code rate R_{RS} given by:

$$R_{RS} = \frac{K}{N}$$

The R-S code words are subsequently interleaved and randomized, which are non-expanding operations (rate equal to one). The interleaved and randomized R-S code words are grouped into blocks of L code words to form an FEC frame. A frame synchronization sequence of s bits is appended to each L code word frame. This additional s bit sync word produces a framing rate loss R_{Frame} given by:

$$R_{Frame} = \frac{\lceil L \cdot N \cdot m \rceil}{\lceil L \cdot N \cdot m + s \rceil}$$

The resultant frames are supplied as the input to the inner trellis code. Trellis groups are formed by serializing the input frames to form groups of five QAM symbols of q bits per symbol, where each of two bits in the five QAM symbols are encoded by a rate 1/2 binary convolutional coder and subsequently punctured to rate 4/5. Thus two of each of the q bits in the five QAM symbol trellis group are rate 4/5 coded for a total of 10 coded bits, and the remaining q-2 bits in each of the 5 QAM symbols trellis group are uncoded. The trellis code rate $R_{Trellis}$ is therefore determined as:

$$R_{Trellis} = \frac{5(q-2) + 5(2)(4/5)}{5q} = \frac{\lceil 5q - 2 \rceil}{5q}$$

The overall concatenated FEC code rate R_{FEC} is given by the product of the code rate of the individual coding procedures just described as:

$$R_{FEC} = R_{RS}\, R_{Frame}\, R_{Trellis}$$

Substituting the above derived code rates yields:

$$R_{FEC} = \frac{K}{N} \cdot \frac{\lceil L \cdot N \cdot m \rceil}{\lceil L \cdot N \cdot m + s \rceil} \cdot \frac{\lceil 5q - 2 \rceil}{5q}$$

The information bit rate R_I is determined from the channel bit rate R_C by the concatenated FEC code rate as:

$R_I = R_C R_{FEC}$

where the channel bit rate is q times the channel symbol rate with q bits per QAM symbol.

The above derived relationships are tabulated for both 64-QAM and 256-QAM below.

Parameter	**Symbol**	**64-QAM Format**	**256-QAM Format**
RS code symbols	N	128	128
RS information symbols	K	122	122
RS bits/symbol	m	7	7
FEC Frame code words	L	60	88
FEC Frame sync bits	s	42	40
QAM bits/symbol	q	6	8
RS code rate	R_{RS}	0.9531250	0.9531250
Framing rate	R_{Frame}	0.9992194	0.9994930
Trellis code rate	$R_{Trellis}$	0.9333333	0.9500000
FEC concatenated code rate	R_{FEC}	0.8888889	0.9050097
Channel symbol rate	R_S	5.056941 Msps	5.360537 Msps
Channel bit rate	R_C	30.34165 Mbps	42.88430 Mbps
Information bit rate	R_I	26.97035 Mbps	38.81070 Mbps