BBC RD 1977/38

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1974
THE QUEEN'S AWARD
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REPORT

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Research Department, Engineering Division
THE BRITISH BROADCASTING CORPORATION October 1977

BBC RD 1977/38
UDC 621.376.56

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**Summary**

*An outline description is given of equipment which converts two high-quality audio signals into digital form, and digitally compands and codes them into a single time-division multiplex signal with a bit rate of 704 kbit/s. The equipment is primarily intended to operate with a four-phase differential phase-shift keying modem and it incorporates special measures in the transmission-error protection system to allow for the error-extension effects which can occur with this type of modulation. The choice of the bit-rate and the signal format adopted are discussed.*

*The combined audio-coding and modulation equipment is intended for use with a radio link to form a stereo outside-broadcast contribution circuit.*

Issued under the authority of

G.D. Monteath

Head of Research Department

**Research Department, Engineering Division,**
**BRITISH BROADCASTING CORPORATION**

October 1977
(EL-131)

## EXPERIMENTAL 704 KBIT/S MULTIPLEX EQUIPMENT FOR TWO 15 KHZ SOUND CHANNELS

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## 1. Introduction

It is often difficult to connect stereo signals from outside broadcasts into the Radio Network because music lines accurately matched in respect of amplitude/frequency and phase/frequency response are not always available. The problem will be eased when Post Office digital transmission circuits become available. In the meantime, however, a possible solution would be to use a radio link to feed a digitally-coded stereo signal to a suitable point of entry into the Radio Network. The digital signal would also be suitable for transmission on a subcarrier above the video signal on an analogue television link.

A modulator-demodulator (modem) equipment has been developed at the BBC Research Department, which modulates a carrier with a digital signal by using 4-phase differential phase-shift keying (d.p.s.k.).[1] The complementary equipment described in this Report provides a digital, multiplexed, 2-channel audio signal for transmission through the d.p.s.k. modem. Measures are included to protect the programme information against the effects of the type of transmission errors which a 4-phase d.p.s.k. system can produce.

## 2. Choice of bit-rate

It is advantageous to use as few bits as possible to describe a signal because the bandwidth of the resulting binary digital signal is proportional to its bit-rate, and the cost of the outside-broadcast link is increased as bandwidth requirements increase.

The BBC 13-channel p.c.m. system which is in service for the distribution of 15 kHz sound programme signals uses a sampling frequency of 32 kHz, with linear coding to an accuracy of 13 bits/sample for each channel. Dither is added to reduce granular distortion and one extra bit is included per sample for error protection.[2] The net bit rate, excluding framing and service bits, is thus 448 kbit/s per audio channel.

Near-instantaneous (NI) digital companding*[3] was used in the 2-channel system described in this Report to reduce the bit rate from over 900 kbit/s which would have been needed for the transmission of two linearly-coded signals. NI companding can reduce the number of bits/sample from 13 to $10^{1}/16$ with virtually no degradation in quality. Moreover, the NI companded signals require only one error-protection bit per two samples (one in each channel)[4] since they are more resistant to the effects of transmission errors than linearly-coded signals.

On this basis therefore the minimum bit-rate that would be required for a stereo signal is about 686 kbit/s, allocated as shown below.

| | kbit/s |
|---|---|
| Sample words, channel 1 | 320 |
| Sample words, channel 2 | 320 |
| Scale-factor bits, channel 1 | 2 |
| Scale-factor bits, channel 2 | 2 |
| Error protection for sample words | 32 |
| Error protection for scale-factor bits | 2 |
| Framing | 8 |
| TOTAL | 686 kbit/s |

It is also desirable to provide some extra capacity in the system for low bit-rate signalling. Possible uses for a low bit-rate channel would be for programme source identification signals or for reporting to a control centre the state of equipment at an unattended site. In the equipment described in this Report, 18 kbit/s are used for low bit-rate signalling making the total bit-rate required 704 kbit/s. There are two reasons for choosing this bit-rate:

(a) 704 is a multiple (11) of 64. Since digital telephone circuits operate at 64 kbit/s per channel it might ultimately be possible to employ groups of such channels for the transmission of sound-programme signals.

(b) By making the total bit-rate a multiple of 32, the data can be sent as 32 sub-frames (each comprising 2 sound sample-words, 1 sample-word parity bit plus 1 supplementary bit for scale-factor, scale-factor protection, framing and low bit-rate signalling) within the 1 ms frame period. Regeneration of sample-words at 32 kHz from 32 sub-frames per millisecond at the receiver is a much more straightforward process than regeneration from the 33 sub-frames per millisecond that would be needed if the bit-rate were not a multiple of 32, the scale-factor, framing and signalling data being carried in its own special sub-frame.

## 3. Frame format

At every sampling instant there are 22 bits available. These bits consist of one 10-bit word from each of the two channels, one sample-word parity bit and one supplementary bit. The 22 bits comprise one sub-frame, and 32 sub-frames

* Near-instantaneous digital companding is a technique in which a block comprising a number of sound-sample words (typically 32 in BBC equipment) is coded to a quantising accuracy of 13, 12, 11 or 10 bits per sample depending on the peak amplitude of the sound signal occurring in the block of 32 samples. A 2-bit scale factor word is sent with each block to indicate the quantising accuracy to the decoder.

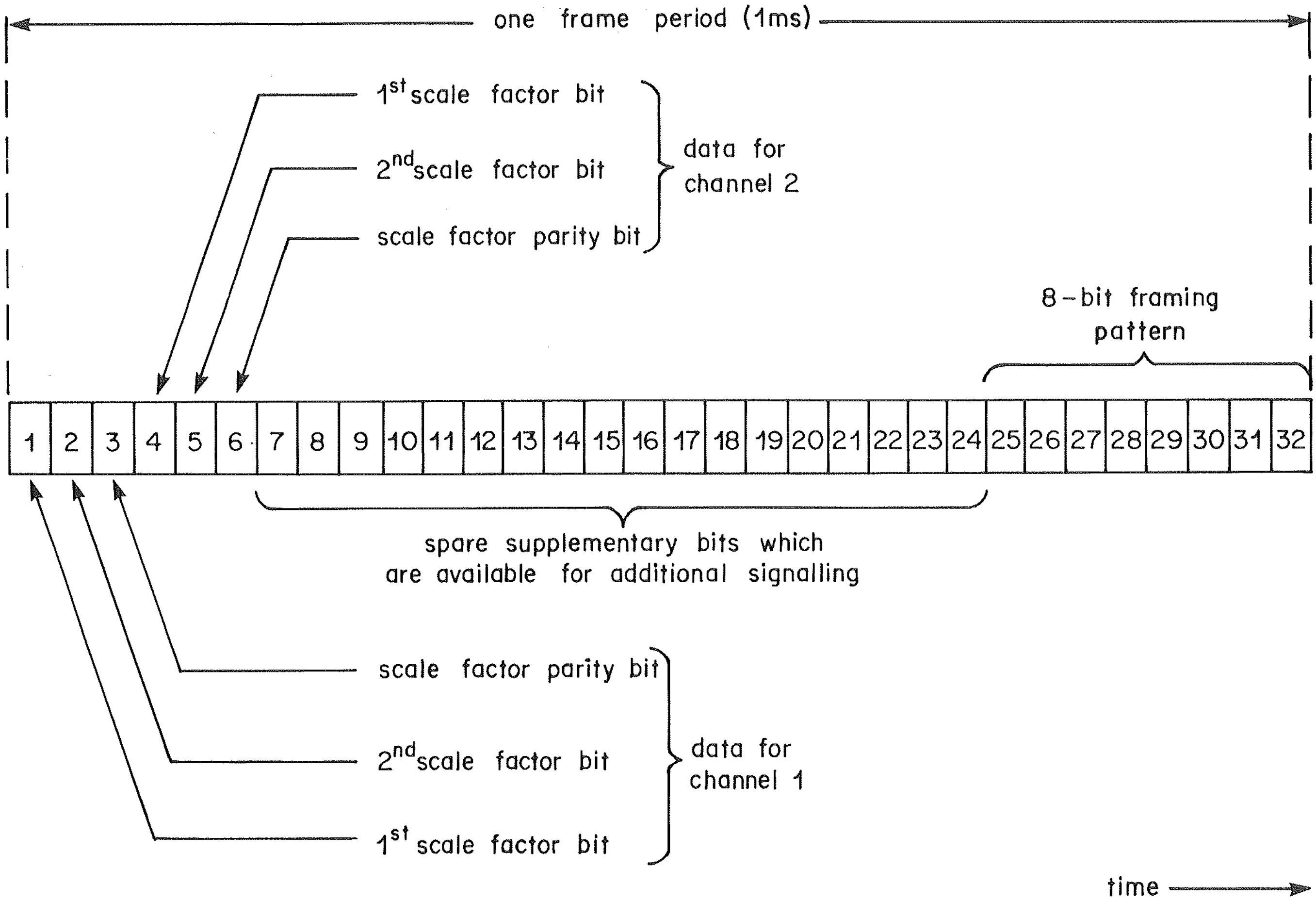


*Fig. 1 - The functions of the distributed supplementary bits in one frame*

make up one frame. The supplementary bits can be scale-factor bits, scale-factor parity bits, framing bits or spare bits for additional signalling.

The functions of all the supplementary bits in one frame (i.e. the 22nd bit of each of the 32 sub-frames which make up one frame) is shown in Fig. 1. Scale-factors and the associated parity checks use the first six supplementary bits, whilst the eight-bit framing pattern is distributed over the last eight sub-frames of each frame. There are thus 18 spare bits in every frame which are used for the 18 kbit/s of additional signalling.

The framing pattern should ideally not be easily imitated by the data; the framing pattern chosen for the 704 kbit/s multiplex equipment was 11010100. The frame

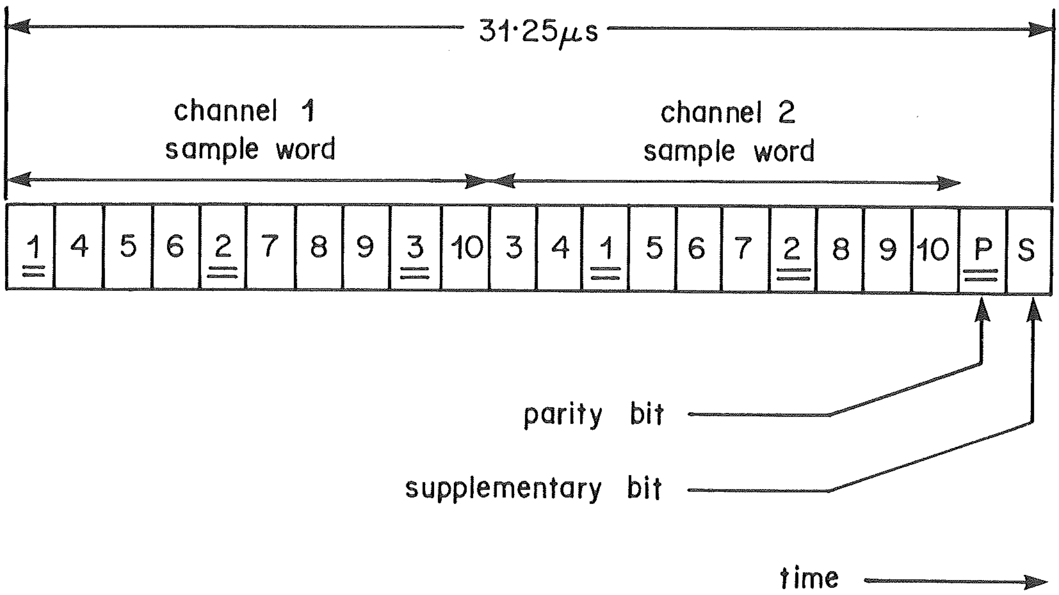


*Fig. 2 - One 22-bit sub-frame of the 704 kbit/s multiplex system*

detection and alignment process has a high degree of immunity to the effects of transmission errors and is described in Section 5.

The sample-word bits in each sub-frame have to be re-ordered to provide the best immunity to transmission errors because the 4-phase d.p.s.k. modulation system for which the 704 kbit/s equipment was designed can produce compound error extensions. A single transmission error can produce more than one error in a group of four consecutive bits in the demodulated binary output.[1] The bits in each sub-frame are therefore re-ordered as shown in Fig. 2, so that the bits involved in the parity group are spaced 3 bits apart thus overcoming the effect of error extension. The bits which are protected by the parity bits are underlined.

The three most significant bits (m.s.b.s) of channel 1, together with the two m.s.b.s of channel 2, are protected by one parity bit, these six bits together forming the parity group. Odd parity checking is used, i.e. the polarity of the parity bit is such that the number of ones in the parity group is always odd. If the signal fails catastrophically to either all ones or all zeroes, parity will be violated and the failure can be detected. Even numbers of errors occurring in the parity group are, of course, not detected by this simple parity checking. The performance of the error protection system is described in Section 6.

With the parity arrangement chosen there is at least one transition from 1 to 0 or 0 to 1 in every sub-frame and this eases the clock-recovery problems in the d.p.s.k. equipment.

## 4. The sending equipment

A simplified block schematic diagram of the sending equipment is shown in Fig. 3.

Before reaching the analogue-to-digital converter (a.d.c.) each audio signal is passed through a 15 kHz low-pass filter, a delay line, a flat limiter, and a variable de-emphasis limiter[5] incorporating 50 μs pre-emphasis. Control voltages for the limiters are developed while the signal is being delayed. The use of a variable de-emphasis limiter with 50 μs pre-emphasis ensures that the audio signal will not overmodulate Band II f.m. transmitters (which incorporate 50 μs pre-emphasis) which may subsequently broadcast the signal.* The limiters in the two programme channels are cross-connected for stereo operation, so that both channels have the same gain. The signal is then de-emphasised by a 50 μs characteristic, pre-emphasised by a CCITT pre-emphasis characteristic and passed through a 15 kHz low-pass filter. CCITT pre-emphasis is beneficial for digital companding and has been agreed within Europe in coding systems to be used for the international exchange of digital sound signals.

The outputs of the a.d.c.s are fed to the compressor. The output of each a.d.c. is a 13-bit serial word in offset (i.e. symmetrical) binary form.**

The compressor converts the 13-bit words to 10-bit words and generates 2-bit scale-factor words. There are, in effect, two compressors, one working in each programme channel and they operate independently of each other but

* Although this equipment is primarily intended for contribution circuits, protecting against overmodulation allows, in principle, the possibility of digital interfacing with the 13-channel p.c.m. stereo distribution system.

** The most significant bit represents the sign of the input signal. The remaining 12 bits represent the magnitude of the signal. The largest negative signal is represented by the code 0111111111111. The largest positive signal is represented by the code 1111111111111.

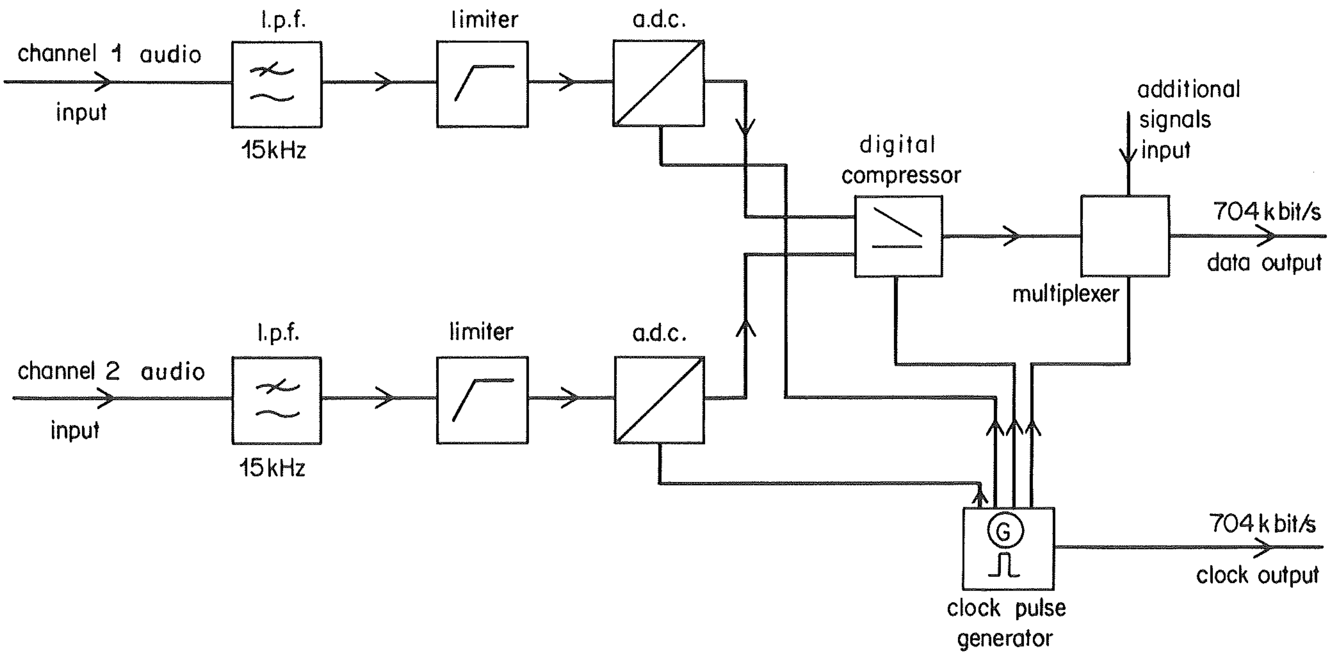


*Fig. 3 - Block schematic diagram of sending equipment*

share the same clock and shift pulses. The 13-bit words are delayed by 32 sample periods (1 ms) while the most significant bits of each word in the complete frame are examined to determine which quantising accuracy to use. If the peak signal level is more than 18 dB below the maximum possible signal, 13-bit quantising is used; if the peak signal level is between 18 and 12 dB below the maximum possible signal, 12-bit quantising is used, and if the peak signal level is between 12 and 6 dB below the maximum possible signal, 11-bit quantising is used. For signals with peak levels within 6 dB of the maximum level, 10-bit quantising is used.

The multiplexer takes the 10-bit words from the compressor and re-orders them in such a way that when added together they will be of the form shown in Fig. 2. The multiplexer also generates parity bits for the data words, scale factor words and the framing pattern, and combines all of these signals to make a 704 kbit/s data stream. The data and a 704 kbit/s clock signal are fed to two output drivers, which give an output of 0 volt for logic 'low' and +1 volt for logic 'high' into 75Ω. Clock transitions occur at the centre of each bit period in the data signal.

The clock pulse generator, which is driven by a crystal-controlled master oscillator at 12·672 MHz (accurate to within ±50 p.p.m.), supplies clock waveforms to the a.d.c.s, the compressor and the multiplexer. The 12·672 MHz waveform is divided down to produce groups of 13 x 6·336 MHz clock pulses to shift the data out of the a.d.c.s and into the compressor, groups of 13 x 704 kHz clock pulses to shift the data through the compressor, and 32 kHz pulses to load the compressor and operate the multiplexer. These signals are in a precisely determined relationship to each other.

Because the data is shifted out of the a.d.c.s in groups of 13 bits, there are periods when the data is stationary. It is during this time that the data is compressed, re-ordered, and formed into parity groups for protection against errors.

The filters, variable de-emphasis limiters and analogue-to-digital converters in the sending equipment are the same as those used in the BBC's prototype 6-channel 2048 kbit/s sound-multiplexing equipment.[6] The digital circuitry uses TTL logic.

## 5. The receiving equipment

A block diagram of the receiving equipment is shown in Fig. 4.* Each block represents a different unit. Data and clock inputs are terminated in 75Ω and converted to CMOS levels. CMOS logic is used in the frame detector and most of the expander to reduce both the number of integrated circuits needed and the power consumption.

The clock pulse generator in the receiver is the same as that used in the sender except that it is not driven from a free-running 12·672 MHz oscillator. Instead, it is driven from a 12·672 MHz crystal oscillator in the phase-locked clock unit.

The phase-locked clock unit and the part of the clock pulse generator which divides the 12·672 MHz down to 704 kHz form a phase-locked loop. The 12·672 MHz oscillator is locked to the incoming 704 kHz clock by comparing the phase of the two 704 kHz signals and making the appropriate adjustments to the oscillator so that the two 704 kHz signals are brought into phase coincidence. Lights are illuminated on the front panel of the phase-locked clock unit to indicate whether the receiver has successfully locked to the incoming 704 kHz clock.

The frame detector detects the framing pattern in the incoming data, re-orders the data bits, checks the parity of the data words, conceals data-word errors and separates the supplementary bits from the bit-stream. It incorporates a

* The frame detector, expander and phase-locked loop were designed largely by C. Gandy.

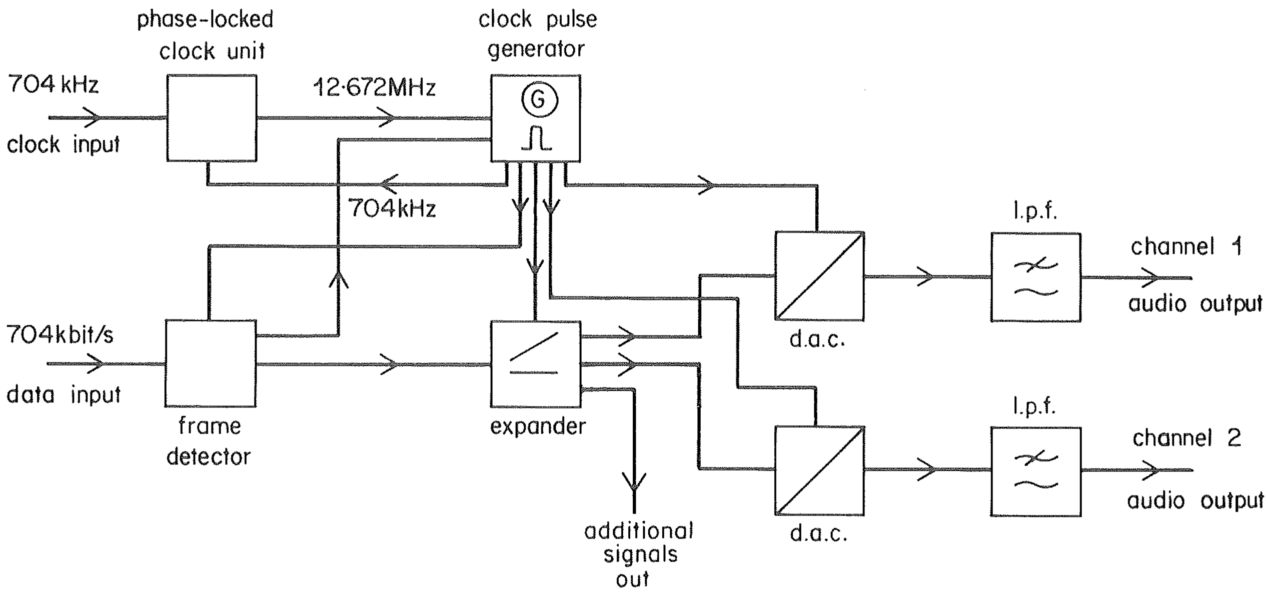


*Fig. 4 - Block schematic diagram of receiving equipment*

7 x 22-bit delay to enable it to look for the 8-bit framing pattern which is spread over 7 sub-frames + 1 bit. The strategy for deciding when frame lock has been achieved is, briefly, as follows.

The frame detector operates in one of two modes; 'LOCKED' mode and 'FRAME-LOCK LOST' mode. When in the locked mode the frame detector looks for framing patterns only where it expects to find them. In the frame-lock lost mode the entire bit-stream is examined. The frame detector contains a 4-bit binary counter which counts up one stage each time a correct framing code is missed, and down one stage, stopping at zero, each time a correct framing code is detected. Once the counter has counted up to state T, known as the 'threshold' the system is said to be in 'FRAME-LOCK LOST' mode. At this stage the frame detector searches the entire bit-stream for a framing pattern. When a framing pattern is found the counter is pre-set to a number, R, known as the residue (R is less than T) and the frame detector returns to the 'LOCKED' mode. It is re-synchronised and works on the assumption that it has found a true framing code, and not a data pattern which happens to be the same as the framing code. The frame detector looks at the bit-stream exactly one frame (1 ms) later. If a framing code is again found the counter starts to count down. If a framing code is not found the counter counts up towards T and the process is repeated. This framing strategy is similar to that developed for the BBC's 120 Mbit/s digital video multiplexing equipment.[7] The numbers R and T are set in binary form on dual-in-line switches to any value between 0 and 15, but with R always less than T.

The frame detector incorporates parity checking for the sample-words. An error in one of the sample-words is detected in the parity detector, which examines each sub-frame of data, and the previous sub-frame is repeated until a correct sub-frame is received. The simple parity check employed in this equipment cannot identify which sample-word contains the error, hence the complete sub-frame is repeated. It is also vulnerable to multiple errors within the sub-frame.

The data and supplementary bits are passed separately to the expandor which separates the data stream into channels 1 and 2, and de-multiplexes the supplementary bits into scale-factor bits, scale-factor parity bits, and additional signalling bits. The expandor then converts the 10-bit digitally companded words into 13-bit p.c.m. words by using the scale-factor word which indicates which bits were removed in the compressor. Missing m.s.b.s are set to '0'. The most significant missing l.s.b. is set to '0' and any other missing l.s.b.s are set to '1'.[4] Thus, when the signal is quantised in the coarsest range, the three missing l.s.b.s are set to 011. If, at any time, a parity violation is detected in a scale-factor word, the scale-factor from the previous frame is held in the expandor.

There is no muting facility provided by the parity checking circuits, but when the error rate becomes high enough to disturb frame locking a 'FRAME-LOCK LOST' mute operates. At the point where this mute operates the impairment caused by errors is very severe. Ideally, a muting circuit fed from the parity detectors would be incorporated so that the system could be muted at lower error rates. This facility was not provided in the present equipment.

## 6. Performance

The experimental 704 kbit/s equipment worked satisfactorily, although there were some minor instrumental problems with the a.d.c.s and d.a.c.s. It is expected that these problems will be overcome during the subsequent development of these converters. The quality of the sound at the output was judged, during listening tests, to be the same as would have been obtained with 13 bits/sample p.c.m.

Tests conducted with the 4-phase d.p.s.k. modem[1] gave satisfactory results. When noise was added at i.f. to the d.p.s.k. signal, random but extended errors were produced in the d.p.s.k. equipment. The performance of the 704 kbit/s system under this condition, with and without error protection, was as expected. The error protection equipment maintained satisfactory operation with error rates up to about 1 in $10^5$. Without error protection, satisfactory operation was obtained at error rates up to about 1 in $10^7$. Although the error protection applied to the two audio channels was slightly different there was no significant difference in the subjective impairment produced on each audio signal, for any constant error rate.

For the values of R and T used, the system did not lose frame lock until the carrier-to-noise ratio at the input to the d.p.s.k. demodulator was 6 dB.

## 7. Conclusions

Experimental equipment has been constructed which will convert two high-quality audio signals into a 704 kbit/s data signal suitable for transmission over a 4-phase d.p.s.k. radio link, and reconvert the signals back into analogue form after reception. The equipment incorporates error protection which enables it to operate satisfactorily at error rates up to 1 in $10^5$; this is obtained with a carrier-to-noise ratio of 13·3 dB at the d.p.s.k. demodulator.[1]

Spare capacity is provided, so that a supplementary data channel could be incorporated for signalling at a low rate (up to 18 kbit/s). Possible uses for this extra capacity might be the identification of programme source, cue information or some kind of security signal.

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Printed by BBC RESEARCH DEPARTMENT, Kingswood Warren, Tadworth, Surrey, KT20 6NP