Flip Chip Challenges

By: **Steve Bezuk, PH.D**.
General Manager, Applied Technology Development and Flip Chip
Kyocera America, Inc.

Introduction

Flip Chip packaging has seen an explosive growth in recent years. Over one billion devices a year are now assembled using flip chip technology. The majority are low lead count devices such as liquid crystal display drivers, watch modules, smart cards, and RFID tags. Recently the trend for higher I/O devices is to turn to flip chip in package (FCIP) as a packaging solution, which is the focus of this article. The growth in this area is driven by the needs of MPU's and high speed and high frequency ASIC's for the computing and communications market. The benefits of flip chip packaging include the following:

- Flip chip technology overcomes wirebond pad pitch limitations,
- Flip chip technology provides electrical designers with many advantages in the design of power and ground distribution on die,
- Flip chip technology provides improved signal integrity for high speed or high frequency designs.

Many MPU & ASIC customers have changed their interconnect technology from wire-bond to flip chip. Some of the most notable include AMD's K6 and K7, Hewlett Packard's PA-RISC, Motorola's Power PC, Sun's UltraSparc II, and Intel's mobile and Coppermine MPU's. Until recently, most of the flip chip activity has been relegated to these larger vertically integrated companies. The key to bringing flip chip to other types of companies is the availability of the logistical infrastructure for flip chip. Within the last two years, the scope of flip chip adopters has broadened to include non-vertically integrated and fabless companies as the support infrastructure has matured. As flip chip packaging expands, many choices are available to the customer such as various bumping technologies, substrate technologies, and the thermal management solutions. The assembler plays a key role in the selection process by providing a manufacturability and reliability viewpoint to this decision. Many challenges still need to be addressed as the market continues to push the limits of flip chip technology. This article will focus on high I/O FCIP devices by following the process flow for the assembly of a FCIP and discussing the challenges and tradeoffs related to selecting processes and materials.

Substrate Technology

Many substrate choices exist for FCIP. Key factors in making a choice of the substrate material for a FCIP are coefficient of thermal expansion (CTE), conductor resistivity, dielectric constant, dielectric loss tangent, and the thermal conductivity of the material. CTE mismatches between the package and the die (first level interconnect) or printed wiring board (PWB) (second level interconnect) play a major factor in the product's reliability. The CTE mismatches generate shear stresses that cause joints to fail. As the operational frequencies rise and supply voltages decrease the electrical characteristics of the substrate materials become much more important. The signal integrity, as it propagates through the package, is a direct function of the conductor resistivity, dielectric constant and the loss tangent. It is important to recognize that the dielectric constant and loss tangent can be strong functions of the frequency. In general, the dielectric loss

tangent is not a strong function of frequency for ceramic packages, while for organic packages the loss tangent is generally larger and can have strong resonances at higher frequencies especially above 1GHz. All of these issues should be considered when choosing a substrate material. Reliability requirements, power dissipation, and operational frequency should be identified and then evaluated against substrate materials properties to choose a substrate material.

		Ceramic		Organic	
	Unit	Alumina	HiTCE	FR-4	BT-resin
Electrical					
Dielectric Constant (1MHz/3.2GHz)		10	5.4/5.4	5.5/—	4.7/—
Dielectric Loss Angle (1MHz/3.2GHz)	($x10^{-4}$)	24	7/20	200/—	100/—
Metallization Sheet Resistance	mΩ /Sq.	10	3	1	1
Thermal					
Thermal Conductivity	W/m°k	18	2	0.2	0.2
Coefficient of Linear Thermal Expansion	1/°C ($x10^{-6}$)	7	12.2	12~14	13~16

FIGURE 1: Substrate material properties

Alumina has long been recognized and accepted as a mature and robust substrate for high density flip chip applications. Alumina's limitations are its low CTE, which creates reliability issues for large outline packages (>35mm) and its high conductor resistance and dielectric constant, which can challenge high power or very high frequency designs.

Organic laminate-based substrates are becoming very popular for FCIP. These are based on high density sequential built up and microvia substrate manufacturing technologies. Organic flip chip packages have low resistance copper interconnects and low dielectric constants. One limitation of organic package technology is its high CTE that creates a large CTE mismatch between the die and substrate. This places heavy demands on the underfill to keep the structure together. Organic materials are also more challenged in environmental reliability tests. Typically they can not pass as demanding a test suite as ceramic packages are able to. Many of the limitations are due to moisture absorption.

Ceramic packaging suppliers are developing new and innovative materials that seek to combine the best feature of ceramic with the best features of organic packages. Kyocera Corporation has developed and is supplying a new Low Temperature Co-Fired Ceramic (LTCC) technology called Hi-TCE[2] to address the current and future requirements for FCIP. Hi-TCE Ceramic has three key discriminators; a TCE of 12.2 ppm/°C, a low dielectric constant of 5.4, and a low resistance copper interconnect system. The high TCE of the material addresses the second level interconnect reliability concerns of ceramic packages. The low dielectric constant and low resistance interconnect of Hi-TCE packages are equivalent to those of organic packages, while its reliability is equivalent to that of ceramic packages. More innovations such as this will be required to meet future technology needs of the industry.

Bumping Technology

Perhaps the key enabling advancement to the flip chip infrastructure was the creation of viable flip chip bumping subcontract service providers. FLIP CHIP Technologies, Unitive, Aptos and several newcomers have provided a comprehensive set of flip chip bump services. High melting point solder bumps (~350C reflow) such as 95/5, and 90/10 Lead/Tin compositions are available, as is eutectic 63/37 (~220C reflow). Figure 2 illustrates the most common bumping technologies.

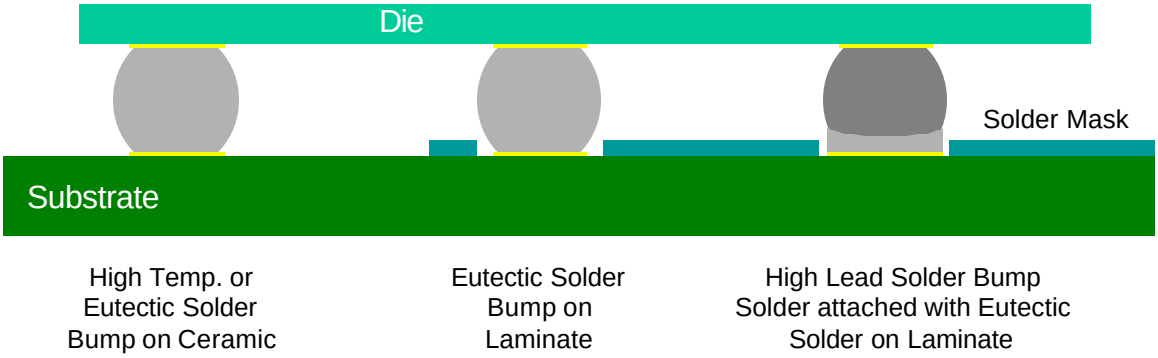

FIGURE 2: Solder bump technologies

Wafer bumping services also have available processes to redistribute wirebond patterns into flip chip compatible bumped die using added metal routing layers. This permits die designed for wirebond assembly to be converted to flip chip devices.

A major challenge for bumping contractors is to maintain dimensional stability of the solder bumps as pitches shrink. Solder bump volume and its corresponding effect on bump coplanarity have a strong effect on flip chip process yield, resulting in opens or shorts in the solder joints.

Passive Component Attach

Many of the products that require flip chip also have a large number of passive components (8 or more are not uncommon) that need to be attached to the substrate. The number, variety, and size of the components used require the assembler to become expert at SMT assembly. Solder paste must be applied to the package to attach these capacitors to the substrate. Pastes matching the flip chip bump composition allow for a single pass reflow of the passives and die. Common methods of applying solder paste are automated dispensing, through a needle or a pogo type valve, or by screening the paste. Screening, albeit the fastest method, has its own difficulties due to its parallel nature of operation. Multiple substrates must be held and aligned simultaneously, which is a difficult task not well handled by current solder screeners in an automated line. In addition, the flip chip site must be kept free from contamination during the screening process.

The assembler must be able to accommodate multiple configurations and sizes of capacitors. Common configurations include two terminal capacitor down to 0402, multiple terminal IDC types, and flip chip style LICA capacitors. One challenge for the future is the placement of very small 0201 capacitors.

Flip Chip Attachment

Equipment for the placement of flip chips is in it's third generation. Equipment is available to place devices with bump pitches down to 150um on 20mm die. The ability to accomplish such high accuracy placement in a high volume manufacturing environment depends more on the vision system and the dimensional tolerance of the package than on the mechanical accuracy of the placement tool. The accuracy of placement is only as good as what the vision system "sees." Vision and lighting systems must be adjusted to account for changes in substrate coloring, surface textures, reflectivity, and substrate transparency. These variables all affect what the vision system sees and therefore the calculated position of the die and package in space. The correct use of fiducials can simplify the vision process. The assembler should be included early in the substrate design process to identify vision requirements and include them in the design or the

assembly yield may suffer. Also, the importance of the dimensional tolerances of the pad positions and size and their effects on bump yields can not be overemphasized.

Increasing throughput for flip chip placement is a practical challenge for future generations of equipment. Practical throughputs are currently ~1000CPH when working with large complex die, and 25% to 50% slower if die are fluxed on the system. Technology is available for fluxing upstream of the flip chip attach equipment on less expensive equipment. Fluxing options include dispensing, brushing, pad stamping, and non-contact jet spray fluxing.

Reflow

Many furnace technologies exist for reflowing flip chip devices. IR, resistively heated tunnel, and convection furnaces are all capable of reflowing flip chip devices. This is the step that gives flip chip one of its major benefits, the formation of all connections to the package in one simple high yield solder reflow step. If done poorly this same simple solder reflow step can create expensive junk very quickly. Few options are available for rework after reflow. Reflowing flip chip devices requires that the reflow furnace provide stable control of the temperature and atmosphere in the furnace. An oxygen sensor is highly recommended to ensure tight process control.

No-clean fluxes have become available for both eutectic and high temperature reflow solders. These fluxes require careful control of reflow profiles to minimize flux residue. If necessary, flux residue cleaning can be accomplished using either a centrifugal cleaner or a pressurized forced flow cleaner. Cleaning typically requires a break in an automated line.

High frequency devices place an added challenge on flip chip placement and reflow. Controlling the gap between the die and the substrate after reflow becomes increasingly important in this situation to maintain transmission line characteristics across the flip chip connection required for signal integrity. Currently the gap is established by the dimensional tolerance of the solder balls and the substrate pads that do meet the needs of very high frequency devices.

Underfill Processing

Underfill is a necessary process for most flip chip assemblies. The shear stress generated by the CTE mismatch between the chip and the substrate leads to early life fatigue failure in the solder joints. Underfilling the flip chip assembly with a high modulus epoxy can minimize the stress, increasing the assembly life up to 50X. The downside of underfilling is that it causes a major bottleneck in the flip chip assembly line. For large die, the flow times can be several minutes. Underfilling is a slow process governed by capillary flow of material under the die. As such, it is affected by the gap between the die and substrate, the bump pattern, the substrate temperature and gradients, viscosity of the underfill, flux contamination, and dispense pattern. Controlling the quality of the underfill dispense, especially voids which can adversely affect reliability, requires understanding and optimizing many material and process parameters. Voids in the underfill, for example, can be caused not only by flux contamination but also by the dispense pattern, volume control, bump pattern and cure profile.

Challenges for materials suppliers are to shorten flow and cure times as well as to design materials with more tolerance for process parameter variation. No-flow underfills are new materials that show promise for significantly reducing assembly cycle time. These materials act as the reflow flux and then cure into the underfill at the same time, completely eliminating the traditional underfill process step.

Thermal Solutions

Power dissipation is a very important consideration when designing a flip chip packaging solution. When the semiconductor industry migrated from Bipolar to CMOS technology power

dissipation issues were minimized. This provided only a brief ten year reprieve. Power's of 50-100W are again an issue. An advantage of flip chip is that it provides access to the backside of the die to remove heat through a low thermal resistance interface to the lid/heatspreader.

The thermal solution usually involves a lid, lid seal adhesive, and a thermal compound between the backside of the die and the lid although direct lid attach (DLA) to the back of the die is an option. Lids can be made from many materials such as copper, aluminum, AlSiC, AlN, CuW, and alumina. The lids will have a CTE mismatch with both the substrate and the silicon die. This mismatch places restrictions on suitable materials for the lid seal and the thermal interface. Low modulus materials help mediate the CTE mismatch with the substrate as well as the die. Although many options are available, acceptable options dwindle quickly as the power dissipation exceeds 25W, particularly in air-cooled environments.

High frequency devices place added complications on the design of a thermal solution. Some device designs are sensitive to any metal near the die and require non-conductive lid solutions such as AlN or alumina. Other designs may require a complete shield of grounded metal around the die that requires not only a metal lid but also electrically conductive adhesives and thermal interfaces.

There are many challenges for new materials development for high power and high frequency devices for thermal solutions in the future. Electrically conductive and non-conductive low modulus adhesives and high thermal conductivity interface materials are needed.

Sphere Attach

The majority of FCIP are also BGA's. The BGA interconnect can be made very dense. Pitches of 0.5mm are currently in production for low I/O CSP's. Common pitches on ball grid arrays are determined more by the design constraints and the cost of the PWB on which they are assembled than by the technical capabilities of the manufacturing equipment. Routing high I/O package second-level connections in a cost-effective way using current PWB technology limits the typical ball pitch to 1.27 and 1.0mm for FCIP components. The most common BGA interconnect styles include the following:

- Eutectic solder spheres
- D-BGA[2] (eutectic-like solder sphere alloy with recessed package contact pad)
- C-BGA[3] (90/10 solder spheres, attached to the package with eutectic solder)

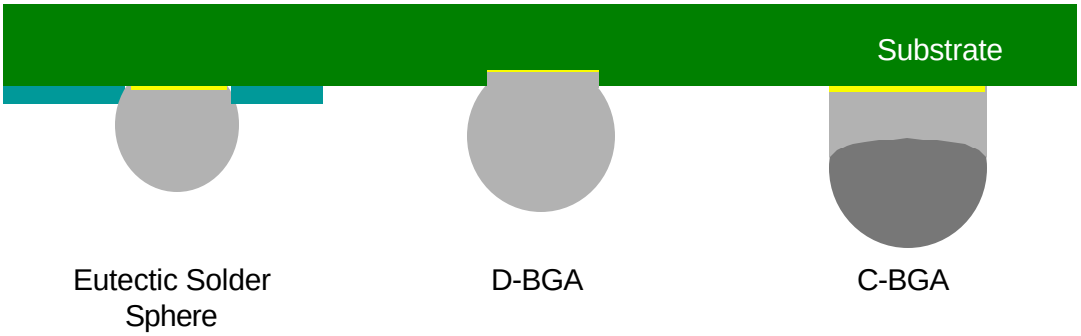

FIGURE 2: BGA technologies

Eutectic solder spheres are used on organic packages. Ceramic packages can be manufactured using either D-BGA or C-BGA technology, with D-BGA technology providing enhanced

reliability. Hi-TCE ceramic packages can be manufactured with eutectic solder spheres or C-BGA technology, which provides enhanced reliability.

The variety of sphere-attach processes leads to many manufacturing equipment challenges. Holding and aligning multiple packages for the subsequent application of flux or solder paste is not a simple task. Most solder sphere-attach equipment is designed to handle strips of PBGA parts where the issue is not relevant. Most equipment is also not designed to screen the solder paste required by both the D-BGA and C-BGA processes.

One of the future challenges in BGA technology will be to manage the gap between the package and the PWB to improve reliability. Controlling the gap will also allow the management of the interconnects' high frequency transmission line properties.

FCIP has an exciting future. Many challenges exist today to provide solutions to customers' current needs. The MPU and communications markets, the latter driven by the ever increasing bandwidth needs of the internet, will continue to push the packaging community to develop more innovative solutions. New materials and processes will continue to be needed in many areas of flip chip technology to maintain its place as an effective solution to industry's packaging requirements.

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